

1. Introduction

1.1. Scope

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit GE864-QUAD / PY module.

1.2. Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our GE864 modules.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit's Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

<http://www.telit.com/en/products/technical-support-center/contact.php>

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

<http://www.telit.com>

To register for product news and announcements or for product questions contact Telit's Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.



1.5. Text Conventions



Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.



Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.



Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.6. Related Documents

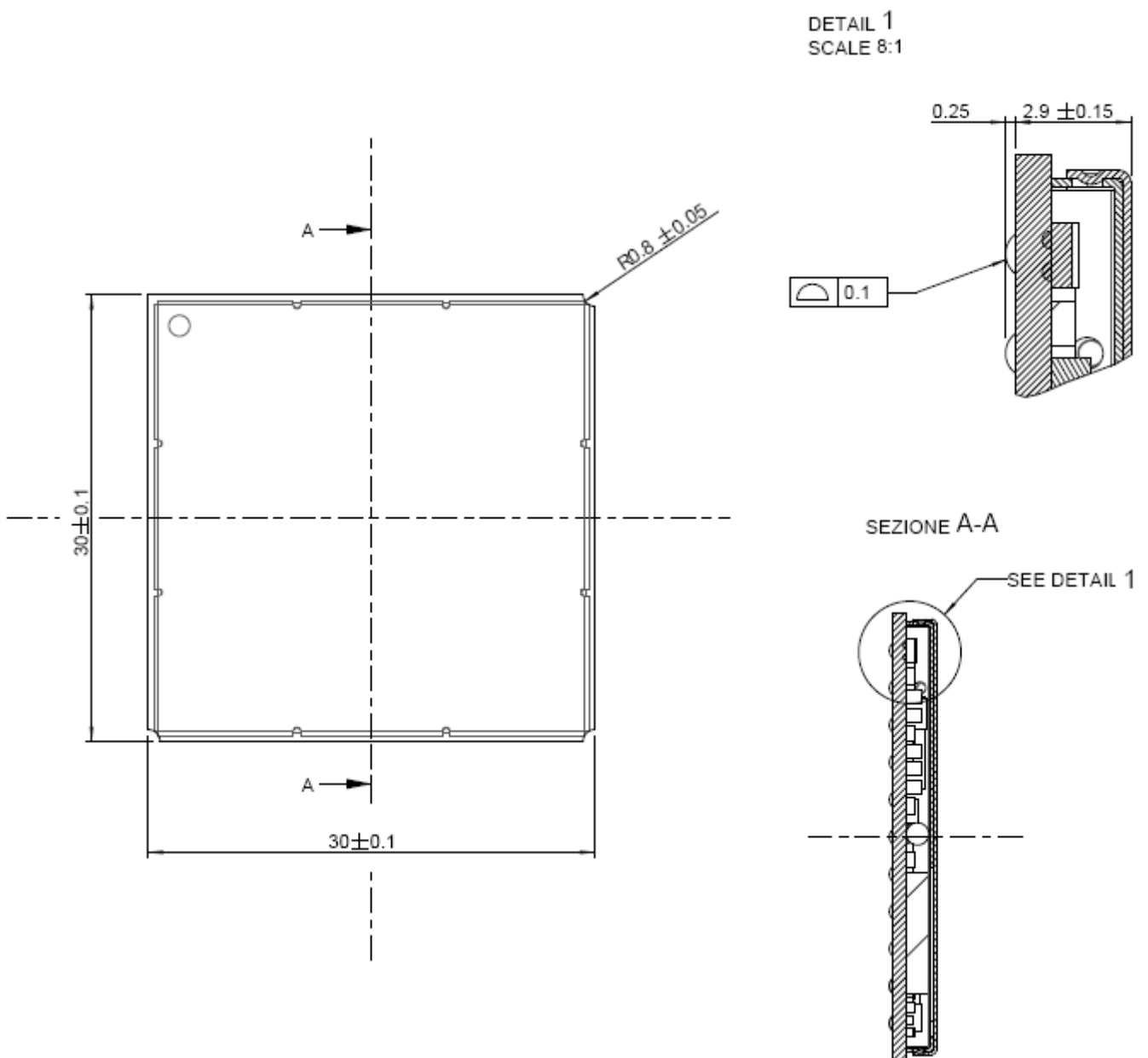
- Telit's GSM/GPRS Family Software User Guide, 1w0300784
- Audio settings application note , 80000NT10007a
- Digital voice Interface Application Note, 80000NT10004a
- GE864 Product description, 80273ST10008a
- SIM Holder Design Guides, 80000NT10001a
- AT Commands Reference Guide, 80000ST10025a



3. GE864 Mechanical Dimensions

The Telit GE864 module overall dimensions are:

- Length: 30 mm
- Width: 30 mm
- Thickness: 2.9 mm



Ball	Signal	I/O	Function	Internal PULL UP	Type
Miscellaneous Functions					
A2	RESET*	I	Reset input		
E2	VRTC	A0	VRTC Backup capacitor		Power
D8	STAT_LED	O	Status indicator led		CMOS 1.8V
G1	CHARGE	AI	Charger input		Power
G2	CHARGE	AI	Charger input		Power
J5	ON_OFF*	I	Input command for switching power ON or OFF (toggle command).	47K	Pull up to VBATT
D5	VAUX1	-	Power output for external accessories		-
L8	PWRMON	O	Power ON Monitor		CMOS 2.8V
L4	Antenna	O	Antenna output – 50 ohm		RF
D7	DVI2_CLK	-	DVI2_CLK (Digital Voice Interface)	4.7K	CMOS 2.8
C6	DVI1_TX	-	Digital Transmitting Data	4.7K	CMOS 2.8
GPIO					
G4	TGPIO_12	I/O	Telit GPIO12 Configurable GPIO		CMOS 2.8V
C2	TGPIO_03	I/O	Telit GPIO03 Configurable GPIO		CMOS 2.8V
B3	TGPIO_04	I/O	Telit GPIO04 Configurable GPIO / RF Transmission Control		CMOS 2.8V
C3	TGPIO_20	I/O	Telit GPIO20 Configurable GPIO		CMOS 2.8V
B4	TGPIO_14	I/O	Telit GPIO14 Configurable GPIO		CMOS 2.8V
D1	TGPIO_11	I/O	Telit GPIO11 Configurable GPIO		CMOS 2.8V
B1	TGPIO_19	I/O	Telit GPIO19 Configurable GPIO		CMOS 2.8V
C1	TGPIO_01	I/O	Telit GPIO01 Configurable GPIO		CMOS 2.8V
K7	TGPIO_18	I/O	Telit GPIO18 Configurable GPIO/ DVI2_RX (Digital Voice Interface)		CMOS 2.8V
H5	TGPIO_17	I/O	Telit GPIO17 Configurable GPIO / DVI2_WA (Digital Voice Interface)		CMOS 2.8V
F5	TGPIO_15	I/O	Telit GPIO15 Configurable GPIO		CMOS 2.8V
K11	TGPIO_08	I/O	Telit GPIO08 Configurable GPIO		CMOS 2.8V
B5	TGPIO_06 / ALARM	I/O	Telit GPIO06 Configurable GPIO / ALARM		CMOS 2.8V
C9	TGPIO_09	I/O	Telit GPIO09 GPIO I/O pin		CMOS 2.8V
E6	TGPIO_02 / JDR	I/O	Telit GPIO02 I/O pin / Jammer detect report		CMOS 2.8V
L9	TGPIO_07 / BUZZER	I/O	Telit GPIO07 Configurable GPIO / Buzzer		CMOS 2.8V
H6	TGPIO_16	I/O	Telit GPIO16 Configurable GPIO		CMOS 2.8V
K10	TGPIO_13	I/O	Telit GPIO13 Configurable GPIO		CMOS 2.8V
K8	TGPIO_05 / RFTXMON	I/O	Telit GPIO05 Configurable GPIO / Transmitter ON monitor		CMOS 2.8V
L10	TGPIO_21	I/O	Telit GPIO21 Configurable GPIO		CMOS 2.8V
E8	TGPIO_22	I/O	Telit GPIO22 Configurable GPIO		CMOS 1.8V (not 2.8V !!)
H3	TGPIO_10	I/O	Telit GPIO10 Configurable GPIO / DVI2_TX (Digital Voice Interface)		CMOS 2.8V
Power Supply					
J1	VBATT	-	Main power supply		Power
K1	VBATT	-	Main power supply		Power
J2	VBATT	-	Main power supply		Power



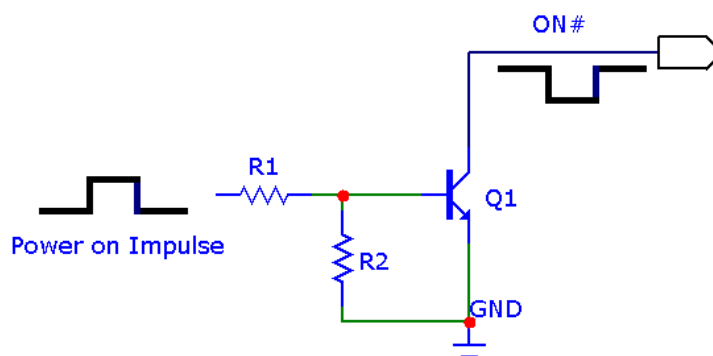
5. Hardware Commands

5.1. Turning ON the GE864-QUAD / PY

To turn on the GE864-QUAD / PY the pad ON# must be tied low for at least 1 second and then released.

The maximum current that can be drained from the ON# pad is 0,1 mA.

A simple circuit to do it is:



NOTE:

Do not use any pull up resistor on the ON# line, it is internally pulled up. Using pull up resistor may bring to latch up problems on the GE864-QUAD / PY power regulator and improper power on/off of the module. The line ON# must be connected only in open collector configuration.

NOTE:

In this document all the lines that are inverted, hence have active low signals are labeled with a name that ends with a “#” or with a bar over the name.

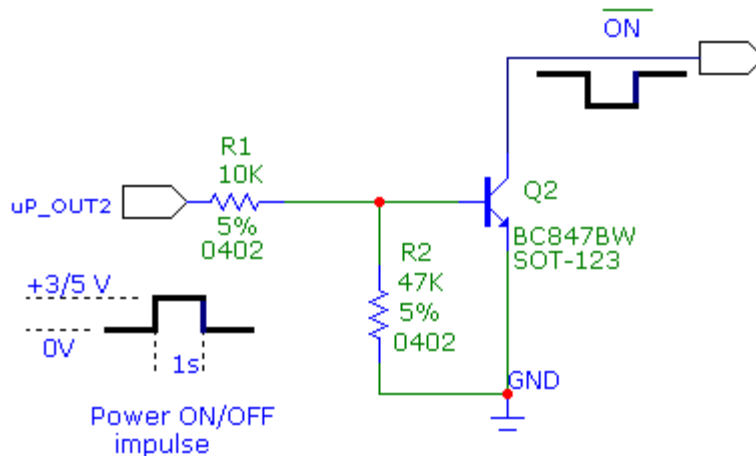
NOTE:

The GE864-QUAD / PY turns fully on also by supplying power to the Charge pad (Module provided with a battery on the VBATT pads).



For example:

Let us assume you need to drive the ON# pad with a totem pole output of a +3/5 V micro controller (uP_OUT1):



Let us assume you need to drive the ON# pad directly with an ON/OFF button:

5.2. Turning OFF the GE864-QUAD / PY

The turning off of the device can be done in two ways:

- via AT command (see GE864-QUAD / PY Software User Guide)
- by tying low pin ON#

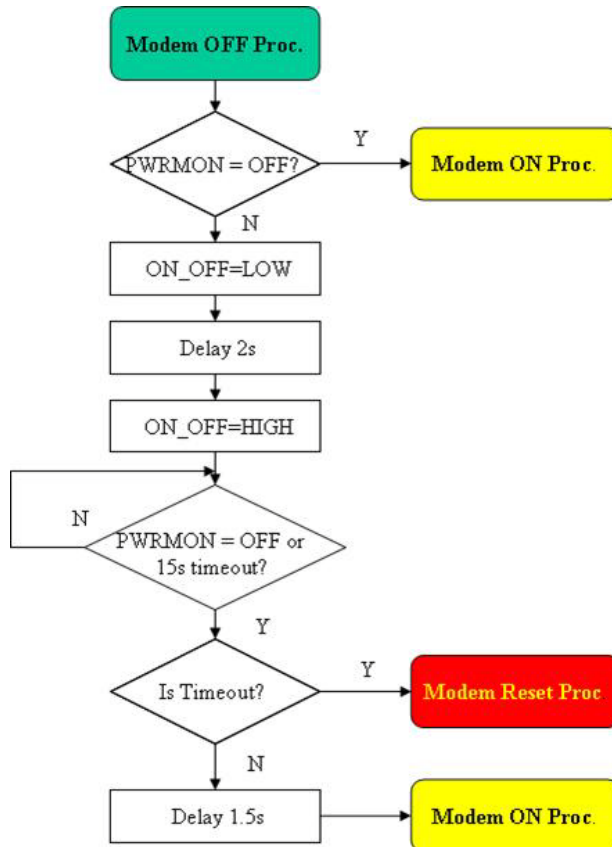
Either ways, when the device issues a detach request to the network informing that the device will not be reachable any more.

To turn OFF the GE864-QUAD / PY the pad ON# must be tied low for at least 2 seconds and then released.

The same circuitry and timing for the power on shall be used.

The device shuts down after the release of the ON# pad.





TIP:

To check if the device has powered off, the hardware line PWRMON must be monitored. When PWRMON goes low, the device has powered off.

5.2.1. Hardware Unconditional Restart



WARNING:

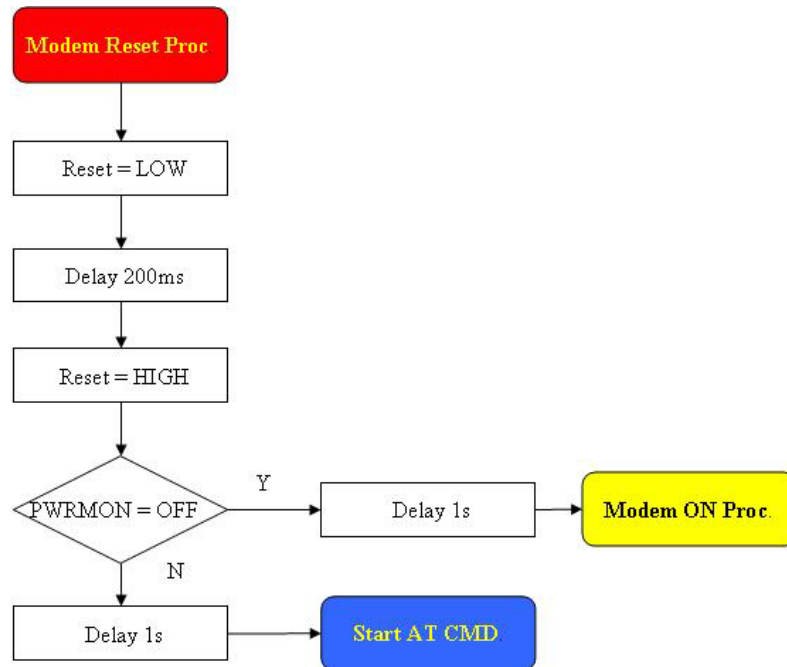
The hardware unconditional Restart must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure to be done in the rare case that the device gets stacked waiting for some network or SIM responses.

To unconditionally restart the GE864-QUAD / PY, the pad RESET# must be tied low for at least 200 milliseconds and then released.

The maximum current that can be drained from the ON# pad is 0.15 mA.

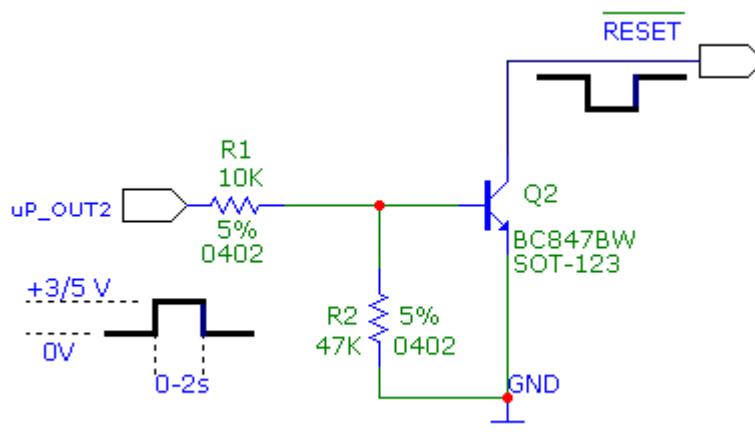


The following flow chart shows the proper Reset procedure:



For example:

Let us assume you need to drive the RESET# pad with a totem pole output of a +3/5 V microcontroller (uP_OUT2):



This signal is internally pulled up so the pin can be left floating if not used.



6. Power Supply

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performances, hence read carefully the requirements and the guidelines that will follow for a proper design.

6.1. Power Supply Requirements

POWER SUPPLY (SW release 7.02.xx4 or older)	
Nominal Supply Voltage	3.8 V
Normal Operating Voltage Range	3.4 V ÷ 4.20 V

POWER SUPPLY (SW release 7.03.x00 or newer)	
Nominal Supply Voltage	3.8 V
Normal Operating Voltage Range	3.4 V ÷ 4.20 V
Extended Operating Voltage Range	3.22 V ÷ 4.50 V



NOTE:

The Operating Voltage Range MUST never be exceeded; care must be taken in order to fulfil min/max voltage requirement.



NOTE:

Overshoot voltage (regarding MAX Extended Operating Voltage) and drop in voltage (regarding MIN Extended Operating Voltage) MUST never be exceeded;

The “Extended Operating Voltage Range” can be used only with completely assumption and application of the HW User guide suggestions.



The table below shows the module's power consumptions:

GE864-QUAD/PY		
Mode	Average (mA)	Mode description
SWITCHED OFF		Module supplied but Switched Off
Switched Off	<26 uA	
IDLE mode		
AT+CFUN=1	19.0	Normal mode: full functionality of the module
AT+CFUN=4	18.2	Disabled TX and RX; module is not registered on the network
AT+CFUN=0 or =5	6.6	Paging Multiframe 2
	4.5	Paging Multiframe 4
	3.3	Paging Multiframe 6
	3.2	Paging Multiframe 8
	2.5	Paging Multiframe 9
CSD TX and RX mode		
GSM900 CSD PL5	237.3	GSM VOICE CALL
DCS1800 CSD PL0	223.8	
GPRS (class 10) 1TX		
GSM900 PL5	264,0	GPRS Sending data mode
DCS1800 PL0	176,0	
GPRS (class 10) 2TX		
GSM900 PL5	473,8	GPRS Sending data mode
DCS1800 PL0	307,8	

The GSM system is made in a way that the RF transmission is not continuous, else it is packed into bursts at a base frequency of about 216 Hz, the relative current peaks can be as high as about 2A. Therefore the power supply has to be designed in order to withstand with these current peaks without big voltage drops; this means that both the electrical design and the board layout must be designed for this current flow.

If the layout of the PCB is not well designed a strong noise floor is generated on the ground and the supply; this will reflect on all the audio paths producing an audible annoying noise at 216 Hz; if the voltage drop during the peak current absorption is too much, then the device may even shutdown as a consequence of the supply voltage drop.



TIP:

The power supply must be designed so that it is capable of a peak current output of at least 2 A.



6.2. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design
- the thermal design
- the PCB layout.

6.2.1. Electrical Design Guidelines

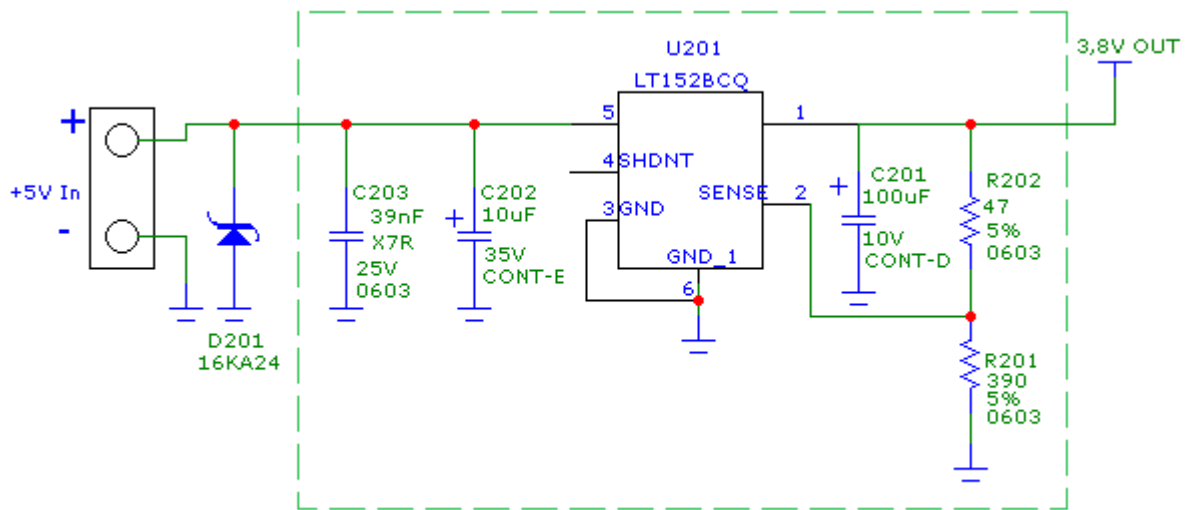
The electrical design of the power supply depends strongly from the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

6.2.1.1. +5V input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence there is not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suited because of the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the GE864-QUAD / PY, a 100 μ F tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode must be inserted close to the power input, in order to save the GE864-QUAD / PY from power polarity inversion.





+5VInput Linear Regulator

An example of linear regulator with 5V input is:

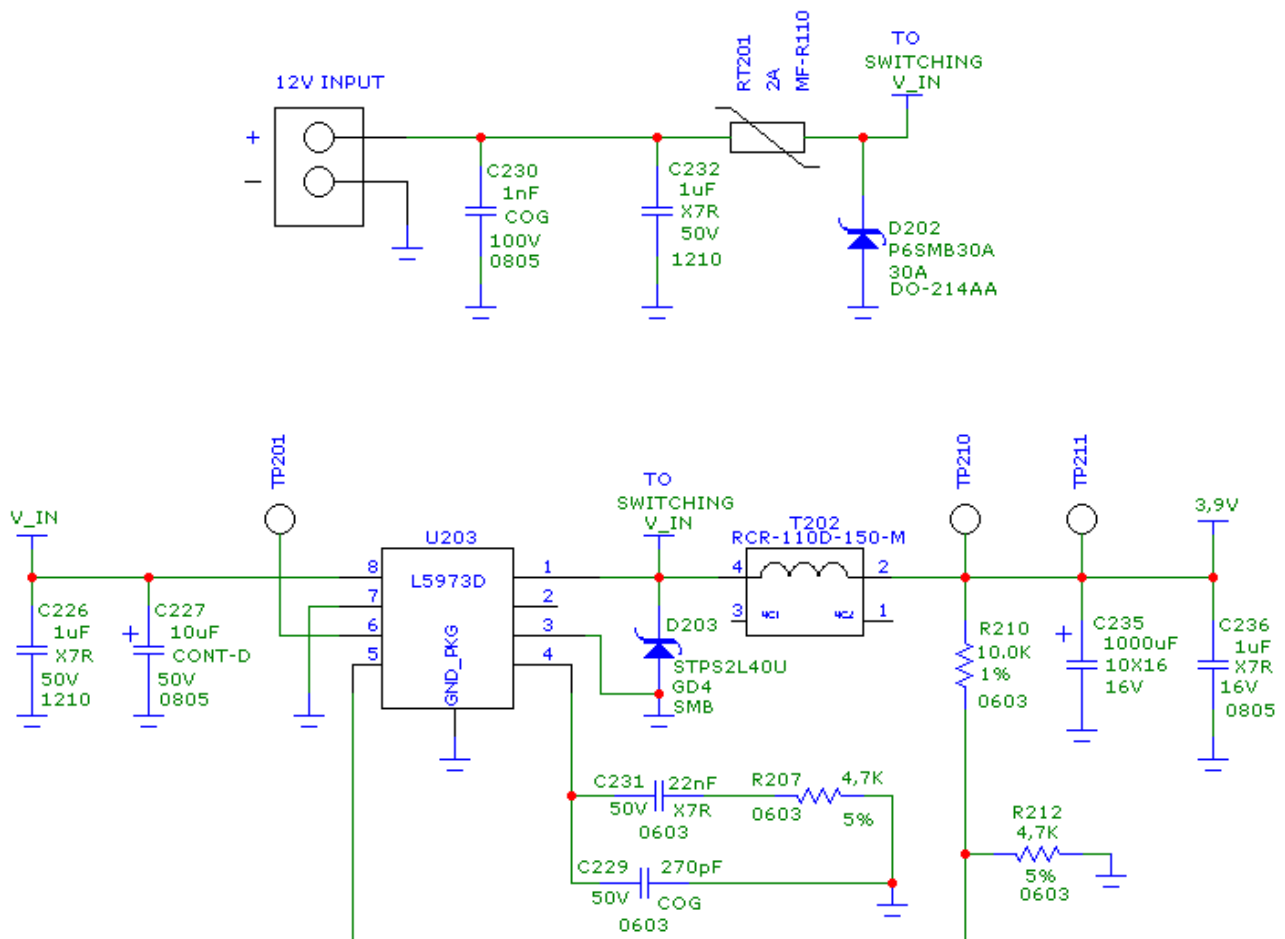
6.2.1.2. +12V input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V; hence due to the big difference between the input source and the desired output, a linear regulator is not suited and shall not be used. A switching power supply will be preferable because of its better efficiency especially with the 2A peak current load represented by the GE864-QUAD/PY.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case the frequency and Switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15.8V and this must be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.



- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- For Car applications a spike protection diode must be inserted close to the power input, in order to clean the supply from spikes.
- A protection diode must be inserted close to the power input, in order to save the GE864-QUAD/PY from power polarity inversion. This can be the same diode as for spike protection.

An example of switching regulator with 12V input is in the below schematic (it is split in 2 parts):



Last but not least, in some applications it is highly desired that the charging process restarts when the battery is discharged and its voltage drops below a certain threshold, GE864-QUAD/PY internal charger does it.

As you can see, the charging process is not a trivial task to be done; moreover all these operations must start only if battery temperature is inside a charging range, usually 5°C – 45°C.

The GE864-QUAD/PY measures the temperature of its internal component, in order to satisfy this last requirement, it is not exactly the same as the battery temperature but in common application the two temperature must not differ too much and the charging temperature range must be guaranteed.



NOTE:

For all the threshold voltages, inside the GE864-QUAD/PY all thresholds are fixed in order to maximize Li-Ion battery performances and do not need to be changed.

NOTE:

In this application the battery charger input current must be limited to less than 400mA. This can be done by using a current limited wall adapter as the power source.

NOTE:

When starting the charger from Module powered off the startup will be in CFUN4; to activate the normal mode a command AT+CFUN=1 has to be provided. This is also possible using the POWER ON.

There is also the possibility to activate the normal mode using the ON_OFF* signal.

In this case, when HW powering off the module with the same line (ON_OFF*) and having the charger still connected, the module will go back to CFUN4.

NOTE:

It is important having a 100uF Capacitor to VBAT in order to avoid instability of the charger circuit if the battery is accidentally disconnected during the charging activity.

6.2.2. Thermal Design Guidelines

The thermal design for the power supply heat sink must be done with the following specifications:

- Average current consumption during transmission @ max PWR level: 500mA
- Average current consumption during transmission @ min PWR level: 100mA



- Average current during Power Saving (CFUN=5): 4mA
- Average current during idle (Power Saving disabled): 24mA



NOTE:

The average consumption during transmissions depends on the power level at which the device is requested to transmit by the network. The average current consumption hence varies significantly.

Considering the very low current during idle, especially if Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.

If we assume that the device stays into transmission for short periods of time (let us say few minutes) and then remains for a quite long time in idle (let us say one hour), then the power supply has always the time to cool down between the calls and the heat sink could be smaller than the calculated one for 500mA maximum RMS current, or even could be the simple chip package (no heat sink).

Moreover in the average network conditions the device is requested to transmit at a lower power level than the maximum and hence the current consumption will be less than the 500mA, being usually around 150mA.

For these reasons the thermal design is rarely a concern and the simple ground plane where the power supply chip is placed can be enough to ensure a good thermal condition and avoid overheating.

For the heat generated by the GE864-QUAD / PY, you can consider it to be during transmission 1W max during CSD/VOICE calls and 2W max during class10 GPRS upload.

This generated heat will be mostly conducted to the ground plane under the GE864-QUAD / PY; you must ensure that your application can dissipate it.



6.2.3. Power Supply PCB Layout Guidelines

As seen on the electrical design guidelines the power supply shall have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performances.

- The Bypass low ESR capacitor must be placed close to the Telit GE864-QUAD / PY power input pads or in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the GE864-QUAD / PY is wide enough to ensure a dropleless connection even during the 2A current peaks.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when the 2A current peaks are absorbed. Note that this is not made in order to save power loss but especially to avoid the voltage drops on the power line at the current peaks frequency of 216 Hz that will reflect on all the components connected to that supply, introducing the noise floor at the burst base frequency. For this reason while a voltage drop of 300-400 mV may be acceptable from the power loss point of view, the same voltage drop may not be acceptable from the noise point of view. If your application does not have audio interface but only uses the data feature of the Telit GE864-QUAD / PY, then this noise is not so disturbing and power supply layout design can be more forgiving.
- The PCB traces to the GE864-QUAD / PY and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur when the 2A current peaks are absorbed. This is for the same reason as previous point. Try to keep this trace as short as possible.
- The PCB traces connecting the Switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for switching power supply). This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).
- The use of a good common ground plane is suggested.
- The placement of the power supply on the board must be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.



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- The power supply input cables must be kept separate from noise sensitive lines such as microphone/earphone cables.



6.2.4. Parameters for ATEX Application

In order to integrate the Telit's GE864 module into an ATEX application, the appropriate reference standard IEC EN xx and integrations shall be followed.

Below are listed parameters and useful information to integrate the module in your application:

- Total capacity: 78.494 μ F
- Total inductance: 10.163 μ H
- No voltage upper than supply voltage is present in the module.
- No step-up converters are present in the module.
- In abnormal conditions, the maximum RF output power is up to 34 dBm max for few seconds.

For this particular application, we recommend the customer to involve TTSC (Telit Technical Support Center) in the design phase of the application.



Furthermore if the device is developed for the US market and/or Canada market, it shall comply to the FCC and/or IC approval requirements:

This device is to be used only for mobile and fixed application. The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. End-Users must be provided with transmitter operation conditions for satisfying RF exposure compliance. OEM integrators must ensure that the end user has no manual instructions to remove or install the GE864-QUAD / PY module. Antennas used for this OEM module must not exceed 3dBi gain for mobile and fixed operating configurations.

7.2. GSM Antenna – PCB Line Guidelines

- Ensure that the antenna line impedance is 50Ω;
- Keep the antenna line on the PCB as short as possible, since the antenna line loss shall be less than 0,3 dB;
- Antenna line must have uniform characteristics, constant cross section, avoid meanders and abrupt curves;
- Keep, if possible, one layer of the PCB used only for the Ground plane;
- Surround (on the sides, over and under) the antenna line on PCB with Ground, avoid having other signal tracks facing directly the antenna line track;
- The ground around the antenna line on PCB has to be strictly connected to the Ground Plane by placing vias once per 2mm at least;
- Place EM noisy devices as far as possible from GE864-QUAD / PY antenna line;
- Keep the antenna line far away from the GE864-QUAD / PY power supply lines;
- If you have EM noisy devices around the PCB hosting the GE864-QUAD / PY, such as fast switching ICs, take care of the shielding of the antenna line by burying it inside the layers of PCB and surround it with Ground planes, or shield it with a metal frame cover.
- If you do not have EM noisy devices around the PCB of GE864-QUAD / PY, by using a strip-line on the superficial copper layer for the antenna line, the line attenuation will be lower than a buried one;



7.3. GSM Antenna – Installation Guidelines

- Install the antenna in a place covered by the GSM signal.
- The Antenna must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter;
- Antenna shall not be installed inside metal cases
- Antenna shall be installed also according Antenna manufacturer instructions.



8. Logic Level Specifications

Where not specifically stated, all the interface circuits work at 2.8V CMOS logic levels. The following table shows the logic level specifications used in the Telit GE864-QUAD / PY interface circuits:

Absolute Maximum Ratings –Not Functional

Parameter	Min	Max
Input level on any digital pin when on	-0.3V	+3.6V
Input voltage on analog pins when on	-0.3V	+3.0 V

Operating Range – Interface Levels (2.8V CMOS)

Level	Min	Max
Input high level	2.1V	3.3V
Input low level	0V	0.5V
Output high level	2.2V	3.0V
Output low level	0V	0.35V

For 1.8V signals:

Operating Range – Interface Levels (1.8V CMOS)

Level	Min	Max
Input high level	1.6V	2.2V
Input low level	0V	0.4V
Output high level	1,65V	2.2V
Output low level	0V	0.35V

Current Characteristics

Level	Typical
Output Current	1mA
Input Current	1uA



9. Serial Ports

The serial port on the Telit GE864-QUAD/PY is the core of the interface between the module and OEM hardware.

2 serial ports are available on the module:

- MODEM SERIAL PORT
- MODEM SERIAL PORT 2 (DEBUG)

9.1. Modem Serial Port

Several configurations can be designed for the serial port on the OEM hardware, but the most common are:

- RS232 PC com port
- Micro controller UART @ 2.8V – 3V (Universal Asynchronous Receive Transmit)
- Micro controller UART@ 5V or other voltages different from 2.8V

Depending from the type of serial port on the OEM hardware a level translator circuit may be needed to make the system work. The only configuration that does not need a level translation is the 2.8V UART.

The serial port on the GE864-QUAD/PY is a +2.8V UART with all the 7 RS232 signals. It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels. The levels for the GE864-QUAD/PY UART are the CMOS levels:

Absolute Maximum Ratings – Not Functional

Parameter	Min	Max
Input level on any digital pad when on	-0.3V	+3.6V
Input voltage on analog pads when on	-0.3V	+3.0 V



Operating Range – Interface Levels (2.8V CMOS)

Level	Min	Max
Input high level V_{IH}	2.1V	3.3V
Input low level V_{IL}	0V	0.5V
Output high level V_{OH}	2.2V	3.0V
Output low level V_{OL}	0V	0.35V



The table below shows the signals of the GE864 serial port:

RS232 Pin Number	Signal	GE864-QUAD / PY Pad Number	Name	Usage
1	DCD – dcd_uart	D9	Data Carrier Detect	Output from the GE864-QUAD / PY that indicates the carrier presence
2	RXD – tx_uart	H8	Transmit line see Note *	Output transmit line of GE864-QUAD / PY UART
3	TXD – rx_uart	E7	Receive line *see Note	Input receive of the GE864-QUAD / PY UART
4	DTR – dtr_uart	B7	Data Terminal Ready	Input to the GE864-QUAD / PY that controls the DTE READY condition
5	GND	A1,F1,H1,L1, H2, L2, J3, K3...	Ground	ground
6	DSR – dsr_uart	E11	Data Set Ready	Output from the GE864-QUAD / PY that indicates the module is ready
7	RTS – rts_uart	F7	Request to Send	Input to the GE864-QUAD / PY that controls the Hardware flow control
8	CTS – cts_uart	F6	Clear to Send	Output from the GE864-QUAD / PY that controls the Hardware flow control
9	RI – ri_uart	B6	Ring Indicator	Output from the GE864-QUAD / PY that indicates the incoming call condition



***NOTE:**

According to V.24, RX/TX signal names are referred to the application side, therefore on the GE864 side these signal are on the opposite direction: TXD on the application side will be connected to the receive line (here named TXD/ rx_uart) of the GE864 serial port and vice versa for RX.



TIP:

For a minimum implementation, only the TXD and RXD lines can be connected, the other lines can be left open provided a software flow control is implemented.

TIP:

In order to avoid noise or interferences on the RXD lines it is suggested to add a pull up resistor (100K Ω to 2.8V)



9.2. RS232 Level Translation

In order to interface the Telit GE864 with a PC com port or a RS232 (EIA/TIA-232) application a level translator is required. This level translator must

- invert the electrical signal in both directions
- change the level from 0/3V to +15/-15V

Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562) , allowing for a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.

The simplest way to translate the levels and invert the signal is by using a single chip level translator. There are a multitude of them, differing in the number of driver and receiver and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).

By convention the driver is the level translator from the 0-3V UART level to the RS232 level, while the receiver is the translator from RS232 level to 0-3V UART.

In order to translate the whole set of control lines of the UART you will need:

- 5 driver
- 3 receiver



NOTE:

The digital input lines working at 2.8VCMOS have an absolute maximum input voltage of 3,75V; therefore the level translator IC shall not be powered by the +3.8V supply of the module. Instead it shall be powered from a +2.8V / +3.0V (dedicated) power supply.

This is because in this way the level translator IC outputs on the module side (i.e. GE864 inputs) will work at +3.8V interface levels, stressing the module inputs at its maximum input voltage.

This can be acceptable for evaluation purposes, but not on production devices.

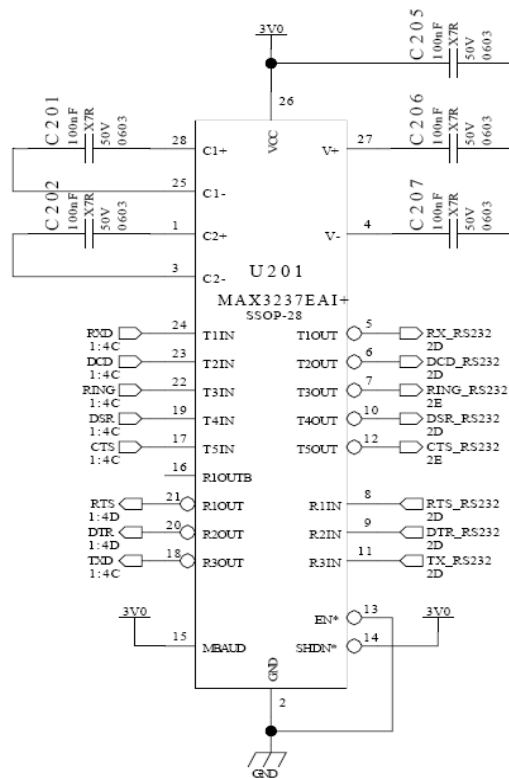
NOTE:

In order to be able to do in circuit reprogramming of the GE864 firmware, the serial port on the Telit GE864 shall be available for translation into RS232 and either it is controlling device shall be placed into tristate, disconnected or as a gateway for the serial data when module reprogramming occurs.

Only RXD, TXD, GND and the On/off module turn on pad are required to the reprogramming of the module, the other lines are unused.

All applicator shall include in their design such a way of reprogramming the GE864.

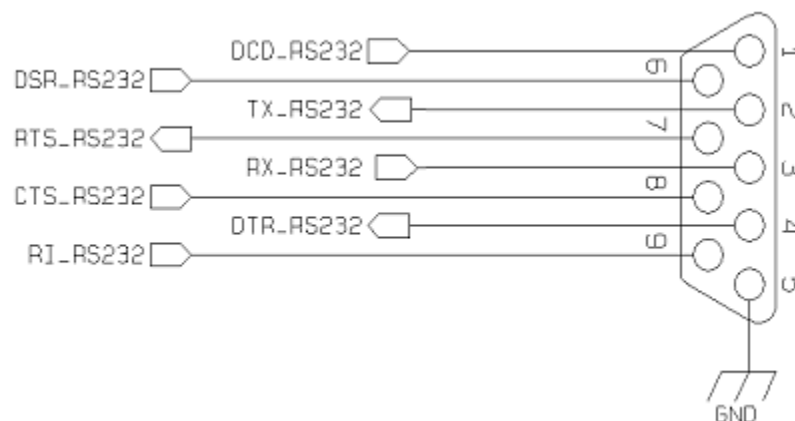




RS232 LEVEL TRSANSULATOR

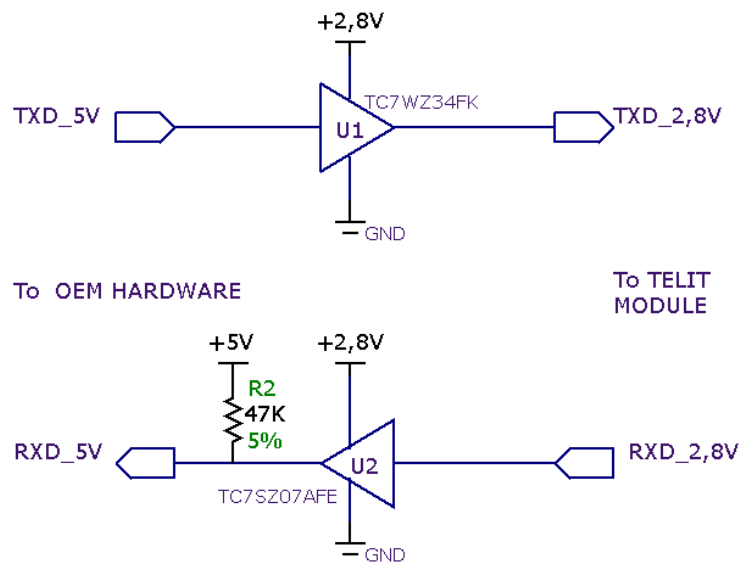
An example of level translation circuitry of this kind is:

The RS232 serial port lines are usually connected to a DB9 connector with the following layout:



9.3. 5V UART Level Translation

If the OEM application uses a microcontroller with a serial port (UART) that works at a voltage different from 2.8 – 3V, then a circuitry has to be provided to adapt the different levels of the two sets of signals. As for the RS232 translation there are a multitude of single chip translators. For example a possible translator circuit for a 5V TRANSMITTER/RECEIVER can be:



TIP:

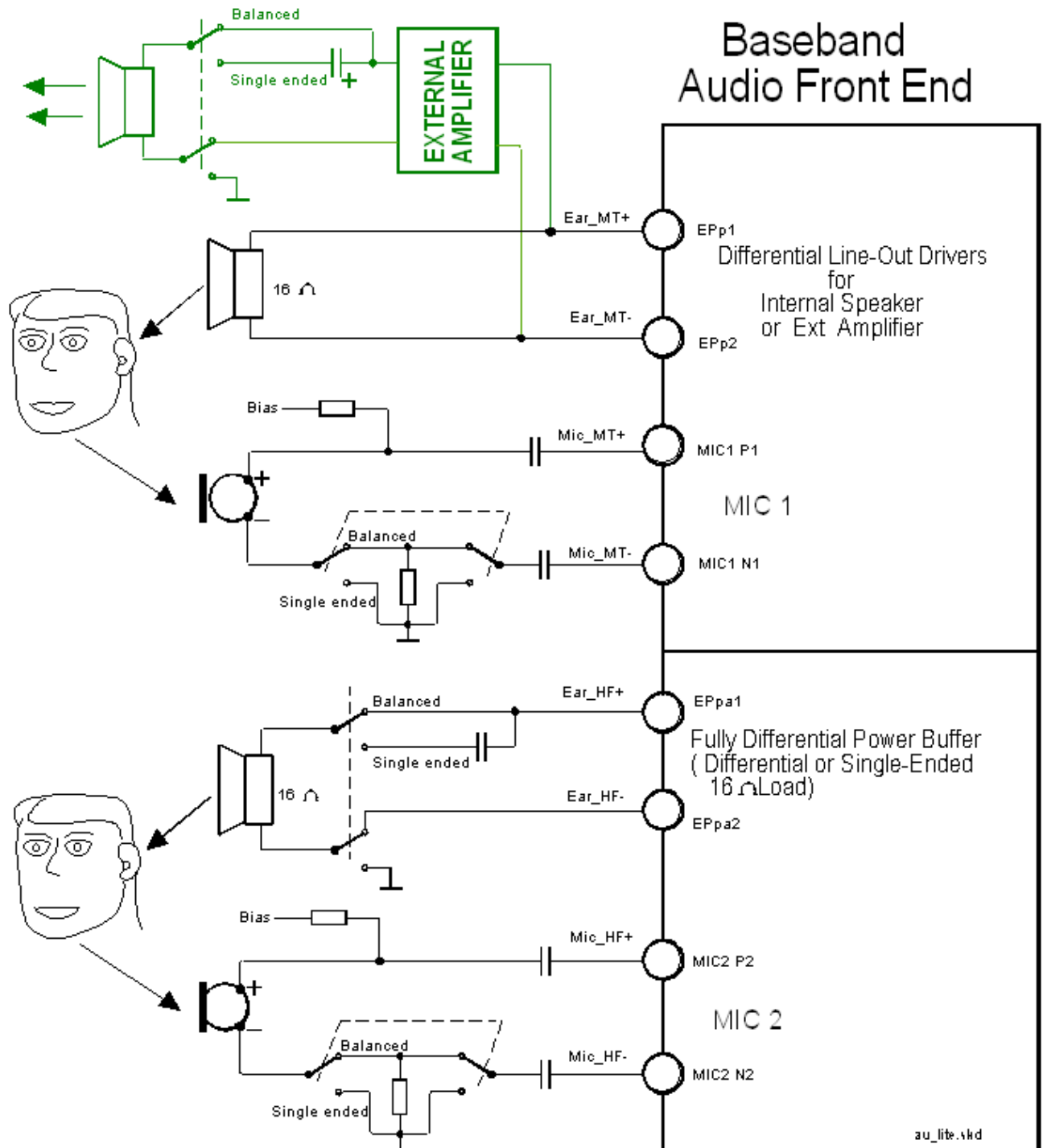
This logic IC for the level translator and 2.8V pull-ups (not the 5V one) can be powered directly from VAUX line of the GE864-QUAD / PY. Note that the TC7SZ07AE has open drain output; therefore the resistor R2 is mandatory.



TIP:

The UART input line TXD (rx_uart) of the GE864-QUAD / PY is NOT internally pulled up with a resistor, so there may be the need to place an external 47KΩ pull-up resistor, either the DTR (dtr_uart) and RTS (rts_uart) input lines are not pulled up internally, so an external pull-up resistor of 47KΩ may be required.





Audio Section Block Diagram



1.2 Electrical Characteristics



TIP: Being the microphone circuitry the more noise sensitive, its design and layout must be done with particular care. Both microphone paths are balanced and the OEM circuitry must be balanced designed to reduce the common mode noise typically generated on the ground plane. However the customer can use the unbalanced circuitry for particular application.

10.1.1. Input Lines Characteristics

"MIC_MT" and "MIC_HF" differential microphone paths	
Line Coupling	AC*
Line Type	Balanced
Coupling capacitor	$\geq 100\text{nF}$
Differential input resistance	$50\text{k}\Omega$
Differential input voltage	$\leq 1,03\text{V}_{\text{pp}}$ @ $\text{MicG}=0\text{dB}$



(*) WARNING : AC means that the signals from the microphone have to be connected to input lines of the module through capacitors which value has to be $\geq 100\text{nf}$. not respecting this constraint, the input stages will be damaged.

WARNING: when particular OEM application needs a *Single Ended Input* configuration, it is forbidden connecting the unused input directly to Ground, but only through a 100nF capacitor. Don't forget that in Single Ended configuration the useful input signal will be halved.



“EAR_MT” Output Lines	
line coupling	AC single-ended DC differential
output load resistance	$\geq 14 \Omega$
internal output resistance	4Ω (<i>typical</i>)
signal bandwidth	150 - 4000 Hz @ -3 dB
max. differential output voltage	$1.31 V_{rms}$ (<i>typical, open circuit</i>)
differential output voltage	$328 mV_{rms} / 16 \Omega / @ -12dBFS$
volume increment	2 dB per step
volume steps	10

“EAR_HF” Output Lines	
line coupling:	AC single-ended DC differential
output load resistance :	$\geq 14 \Omega$
internal output resistance:	$4 \Omega (>1,7 \Omega)$
signal bandwidth:	150 - 4000 Hz @ -3 dB
max. differential output voltage	$1.31 V_{rms}$ (<i>typical, open circuit</i>)
max. S.E. output voltage	$656 mV_{rms}$ (<i>typical, open circuit</i>)
volume increment	2 dB per step
volume steps	10



11. External SIM Holder Implementation

Please refer to the related Telit User Guide :

“80000NT10001a SIM Holder Design Guides”



12. General Purpose I/O

The general purpose I/O pads can be configured to act in three different ways:

- input
- output
- alternate function (internally controlled)

Input pads can only be read and report the digital value (high or low) present on the pad at the read time; output pads can only be written or queried and set the value of the pad output; an alternate function pad is internally controlled by the GE864-QUAD / PY firmware and acts depending on the function implemented. For Logic levels please refer to chapter 7.

The following GPIO are available on the GE864-QUAD and GE864-PY:

Ball	Signal	I/O	Function	Type	Input / output current	Default State	ON_OFF state	State during Reset	Note
C1	TGPIO_01	I/O	GPIO01 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
E6	TGPIO_02	I/O	GPIO02 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		Alternate function (JDR)
C2	TGPIO_03	I/O	GPIO03 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
B3	TGPIO_04	I/O	GPIO04 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		Alternate function (RF Transmission Control)
K8	TGPIO_05	I/O	GPIO05 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		Alternate function (RFTXMON)
B5	TGPIO_06	I/O	GPIO06 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	Pict 01	1	Alternate function (ALARM)
L9	TGPIO_07	I/O	GPIO07 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		Alternate function (BUZZER)
K11	TGPIO_08	I/O	GPIO08 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
C9	TGPIO_09	I/O	GPIO09 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
H3	TGPIO_10	I/O	GPIO10 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
D1	TGPIO_11	I/O	GPIO11 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
G4	TGPIO_12	I/O	GPIO12 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
K10	TGPIO_13	I/O	GPIO13 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
B4	TGPIO_14	I/O	GPIO14 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
F5	TGPIO_15	I/O	GPIO15 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
H6	TGPIO_16	I/O	GPIO16 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
H5	TGPIO_17	I/O	GPIO17 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
K7	TGPIO_18	I/O	GPIO18 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
B1	TGPIO_19	I/O	GPIO19 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
C3	TGPIO_20	I/O	GPIO20 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
L10	TGPIO_21	I/O	GPIO21 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	1		
E8	TGPIO_22	I/O	GPIO22 Configurable GPIO	CMOS 1.8V (not 2.8V !!)	1uA / 1mA	INPUT	0		

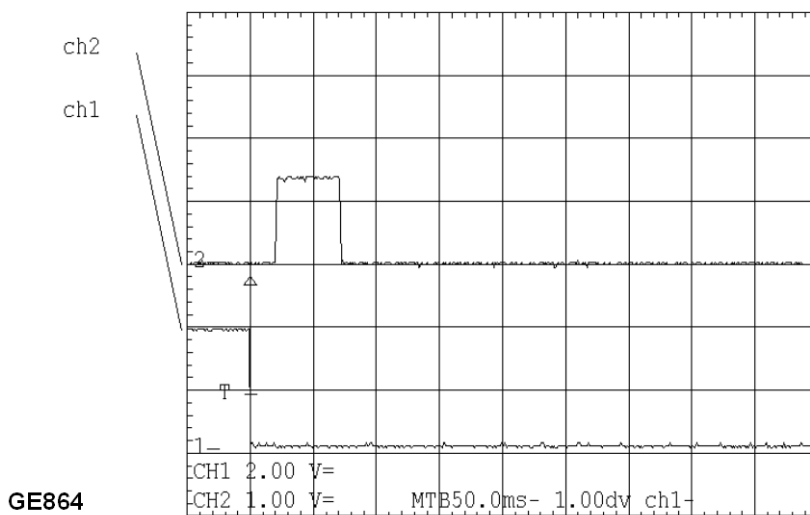


Not all GPIO pads support all these three modes:

- GPIO2 supports all three modes and can be input, output, Jamming Detect Output (Alternate function)
- GPIO4 supports all three modes and can be input, output, RF Transmission Control (Alternate function)
- GPIO5 supports all three modes and can be input, output, RFTX monitor output (Alternate function)
- GPIO6 supports all three modes and can be input, output, alarm output (Alternate function)
- GPIO7 supports all three modes and can be input, output, buzzer output (Alternate function)

ch1: ON_OFF (2sec)

ch2: GPIO 06 [bis]



12.1. GPIO Logic Levels

Where not specifically stated, all the interface circuits work at 2.8V CMOS logic levels.

The following tables show the logic level specifications used in the GE864-QUAD/PY interface circuits:

Absolute Maximum Ratings – Not Functional

Parameter	Min	Max
Input level on any digital pin when on	-0.3V	+3.6V
Input voltage on analog pins when on	-0.3V	+3.0 V

Operating Range – Interface Levels (2.8V CMOS)

Level	Min	Max
Input high level	2.1V	3.3V
Input low level	0V	0.5V
Output high level	2.2V	3.0V
Output low level	0V	0.35V

For 1.8 V signals:

Operating Range – Interface Levels (1.8V CMOS)

Level	Min	Max
Input high level	1.6V	2.2V
Input low level	0V	0.4V
Output high level	1,65V	2.2V
Output low level	0V	0.35V



12.2. Using a GPIO Pad as INPUT

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 2.8V CMOS levels of the GPIO.

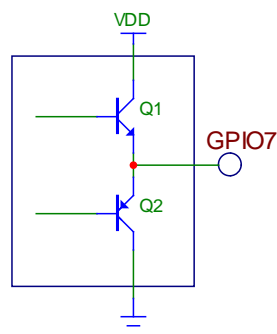
If the digital output of the device to be connected with the GPIO input pad has interface levels different from the 2.8V CMOS, then it can be buffered with an open collector transistor with a 47K pull up to 2.8V.

12.3. Using a GPIO Pad as OUTPUT

The GPIO pads, when used as outputs, can drive 2.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

The illustration below shows the base circuit of a push-pull stage:

12.4. Using the RF Transmission Control GPIO4



The GPIO4 pin, when configured as RF Transmission Control Input, permits to disable the Transmitter when the GPIO is set to Low by the application.

In the design is necessary to add a pull up resistor (47K to VAUX).

12.5. Using the RFTXMON Output GPIO5

The GPIO5 pin, when configured as RFTXMON Output, is controlled by the GE864-QUAD / PY module and will rise when the transmitter is active and fall after the transmitter activity is completed.

For example, if a call is started, the line will be HIGH during all the conversation and it will be again LOW after hanged up.

The line rises up 300ms before first TX burst and will became again LOW from 500ms to 1sec after last TX burst.



12.6. Using the Alarm Output GPIO6

The GPIO6 pad, when configured as Alarm Output, is controlled by the GE864-QUAD / PY module and will rise when the alarm starts and fall after the issue of a dedicated AT command.

This output can be used to power up the GE864-QUAD / PY controlling micro controller or application at the alarm time, giving you the possibility to program a timely system wake-up to achieve some periodic actions and completely turn off either the application and the GE864-QUAD / PY during sleep periods, dramatically reducing the sleep consumption to few μA .

In battery-powered devices this feature will greatly improve the autonomy of the device.



NOTE:

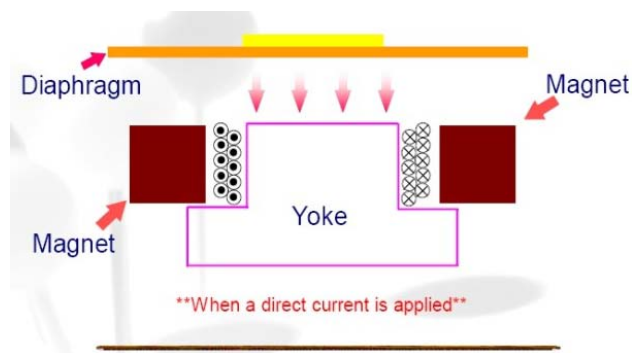
During RESET the line is set to HIGH logic level.



12.8. Magnetic Buzzer Concepts

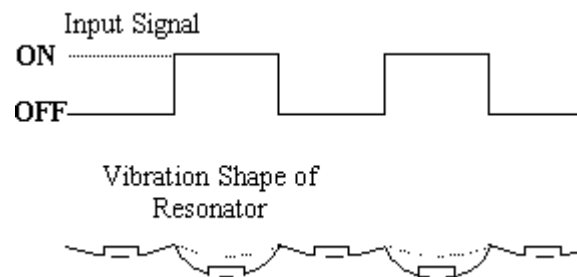
12.8.1. Short Description

A magnetic Buzzer is a sound-generating device with a coil located in the magnetic circuit consisting of a permanent magnet, an iron core, a high permeable metal disk, and a vibrating diaphragm.



Drawing of the Magnetic Buzzer

The disk and diaphragm are attracted to the core by the magnetic field. When an oscillating signal is moved through the coil, it produces a fluctuating magnetic field, which vibrates the diaphragm at a frequency of the drive signal. Thus the sound is produced relative to the frequency applied.



Diaphragm movement

12.8.2. Frequency Behavior

The frequency behavior represents the effectiveness of the reproduction of the applied signals.



Because its performance is related to a square driving waveform (whose amplitude varies from 0V to V_{pp}), if you modify the waveform (e.g. from square to sinus) the frequency response will change.

12.8.3. Power Supply Influence

Applying a signal whose amplitude is different from that suggested by manufacturer, the performance change following the rule:

“if resonance frequency f_0 increases, amplitude decreases”.

Because of resonance frequency depends from acoustic design, lowering the amplitude of the driving signal the response bandwidth tends to become narrow, and vice versa.

Summarizing: $V_{pp} \uparrow \rightarrow f_0 \downarrow$ $V_{pp} \downarrow \rightarrow f_0 \uparrow$

The risk is that the f_0 could easily fall outside of new bandwidth; consequently the SPL could be much lower than the expected.



WARNING:

It is very important to respect the sense of the applied voltage: never apply to the "-" pin a voltage more positive than the "+" pin: if this happens, the diaphragm vibrates in the opposite direction with a high probability to be expelled from its physical position. This damages the device permanently.

12.8.4. Working Current Influence

In the component data sheet you will find the value of MAX CURRENT that represents the maximum average current that can flow at nominal voltage without current limitation.

In other words it is not the peak current, which could be twice or three times higher.

If driving circuitry does not support these peak values, the SPL will never reach the declared level or the oscillations will stop.



12.10. Indication of Network Service Availability

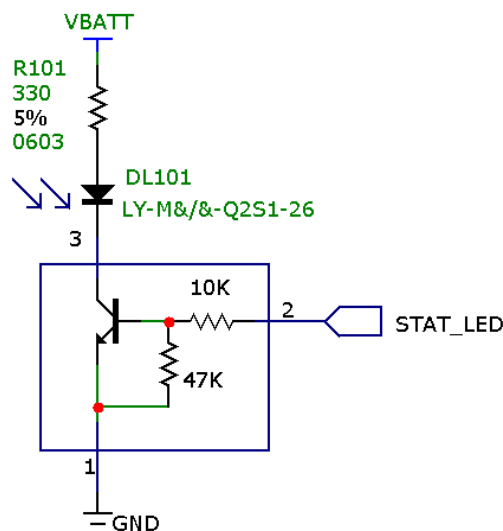
The STAT_LED pin status shows information on the network service availability and Call status.

In the GE864 modules, the STAT_LED usually needs an external transistor to drive an external LED.

Therefore, the status indicated in the following table is reversed with respect to the pin status.

LED status	Device Status
Permanently off	Device off
Fast blinking (Period 1s, Ton 0,5s)	Net search / Not registered / turning off
Slow blinking (Period 3s, Ton 0,3s)	Registered full service
Permanently on	a call is active

A schematic example could be:



12.11. RTC Bypass Out

The VRTC pin brings out the Real Time Clock supply, which is separate from the rest of the digital part, allowing having only RTC going on when all the other parts of the device are off.

To this power output a backup capacitor can be added in order to increase the RTC autonomy during power off of the battery. NO Devices must be powered from this pin.

12.12. VAUX1 Power Output

A regulated power supply output is provided in order to supply small devices from the module.

This output is active when the module is ON and goes OFF when the module is shut down.

The operating range characteristics of the supply are:

Operating Range – VAUX1 power supply

	Min	Typical	Max
Output voltage	2.75V	2.85V	2.95V
Output current			100mA
Output bypass capacitor (inside the module)			2.2 μ F



13. DAC and ADC Section

13.1. DAC Converter

13.1.1. Description

The GE864-QUAD / PY module provides a Digital to Analog Converter. The signal (named DAC_OUT) is available on BGA Ball C7 of the GE864-QUAD / PY module and on pin 17 of PL102 on EVK2 Board (CS1152).

The on board DAC is a 10-bit converter, able to generate a analogue value based a specific input in the range from 0 up to 1023. However, an external low-pass filter is necessary

	Min	Max	Units
Voltage range (filtered)	0	2,6	Volt
Range	0	1023	Steps

The precision is 10 bits so, if we consider that the maximum voltage is 2V, the integrated voltage could be calculated with the following formula:

$$\text{Integrated output voltage} = 2 * \text{value} / 1023$$

DAC_OUT line must be integrated (for example with a low band pass filter) in order to obtain an analog voltage.

13.1.2. Enabling DAC

The AT command below is available to use the DAC function:

AT#DAC[=<enable>[,<value>]]

<value> – scale factor of the integrated output voltage (0..1023 – 10 bit precision)

it must be present if **<enable>=1**

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.



NOTE:

The DAC frequency is selected internally. D/A converter must not be used during POWERSAVING.

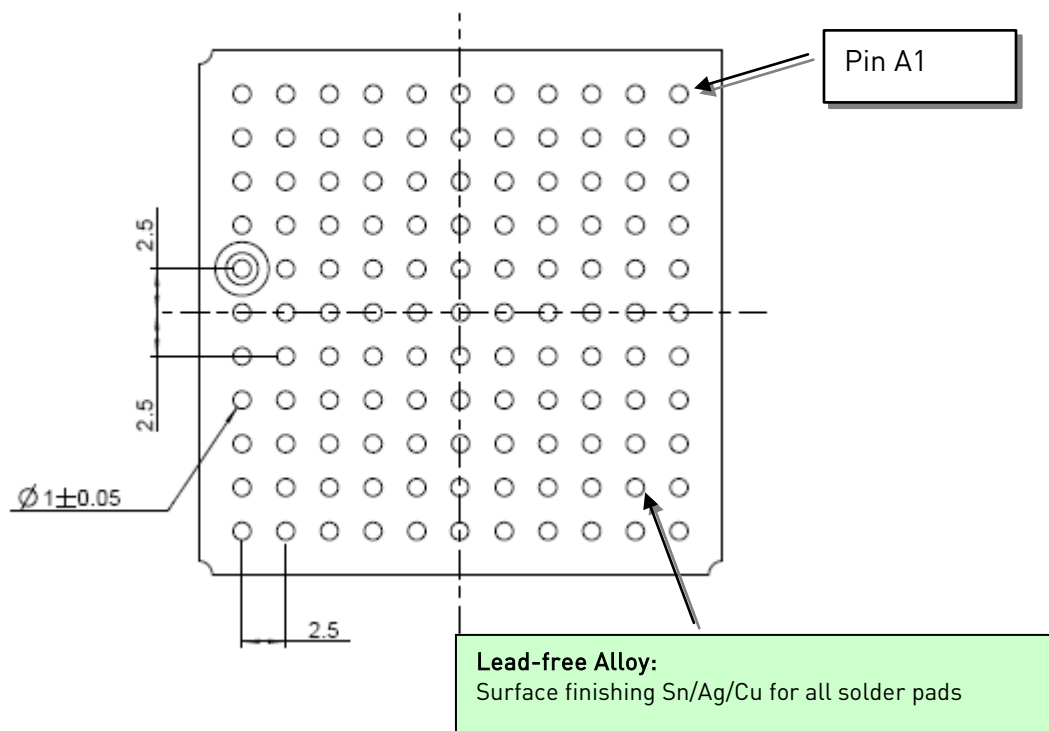


14. Mounting the GE864 on the Board

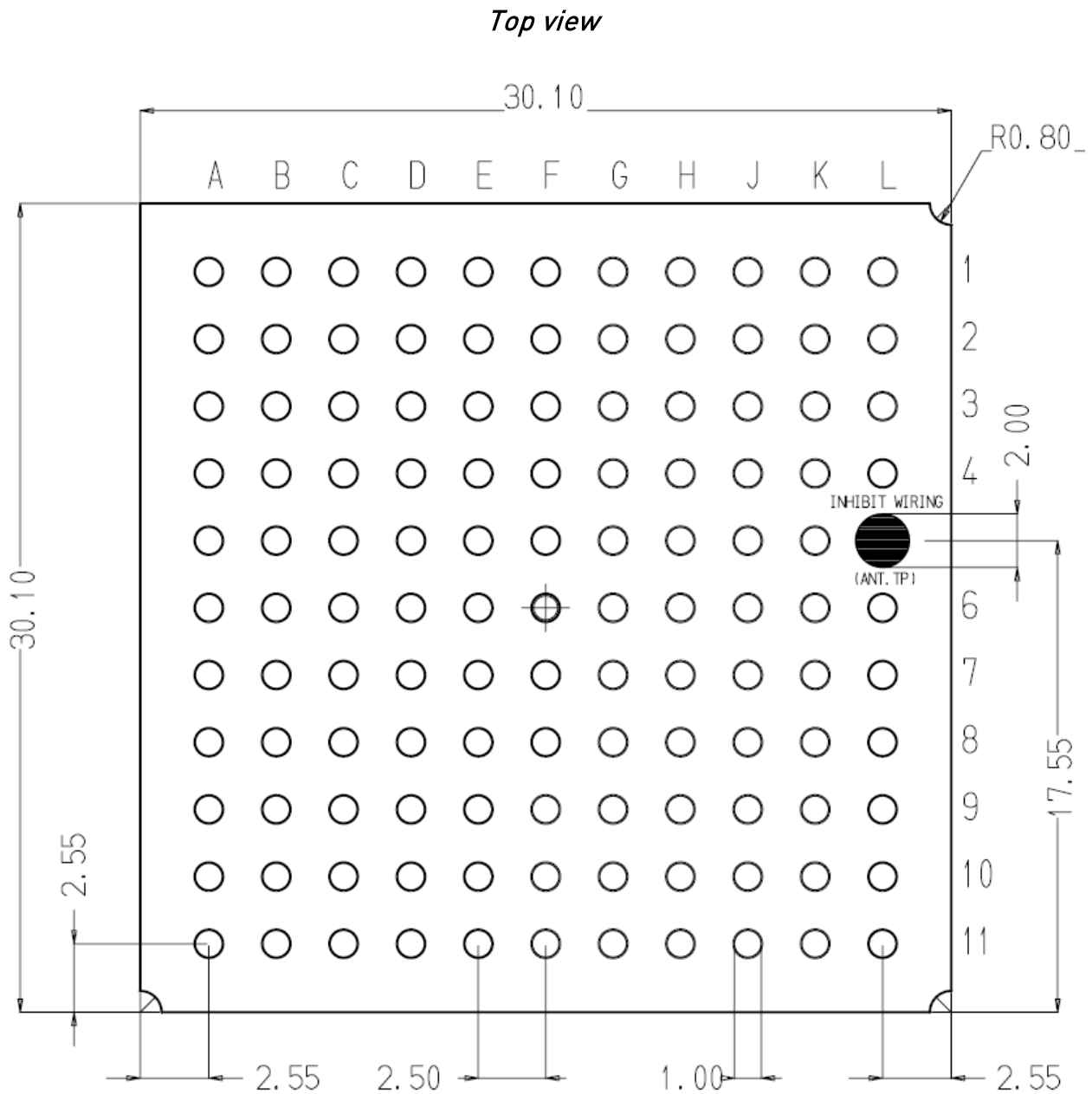
14.1. General

The Telit GE864 modules have been designed in order to be compliant with a standard lead-free SMT process.

14.1.1. Module Finishing & Dimensions



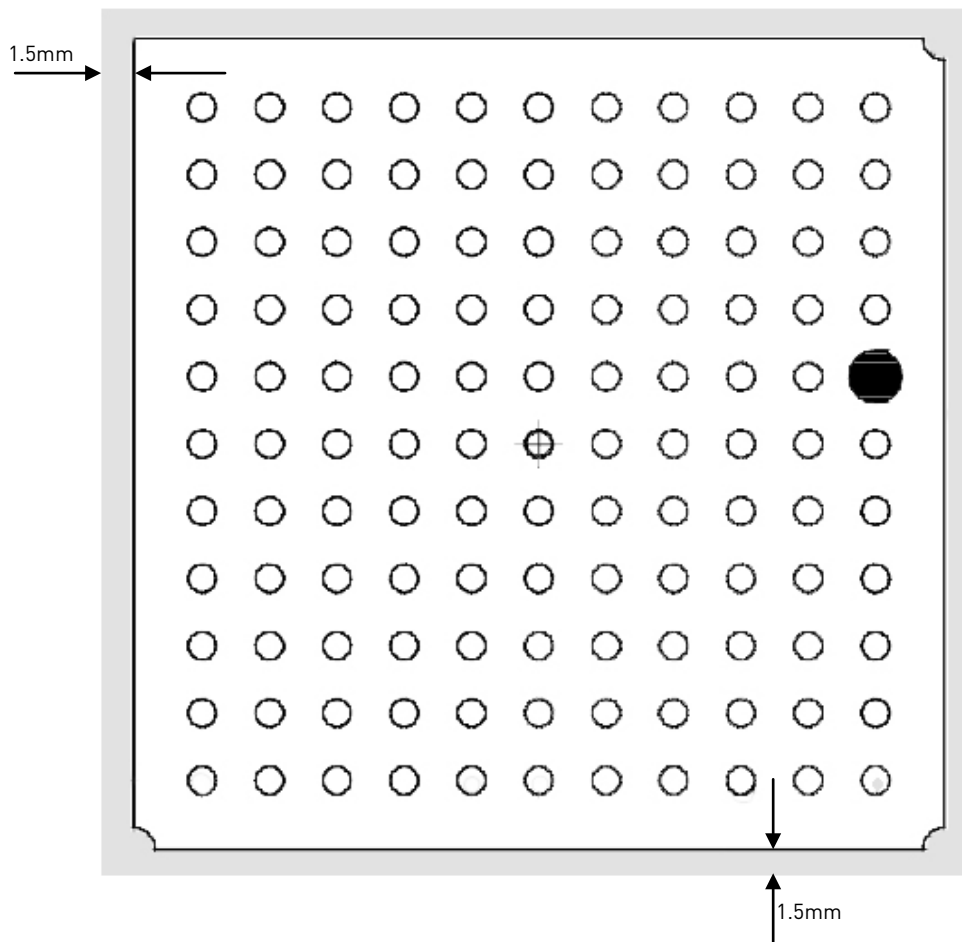
14.1.2. Recommended Foot Print for the Application (GE864)



14.1.3. Suggested Inhibit Area

In order to easily rework the GE864 is suggested to consider on the application a 1.5mm Inhibit area around the module:

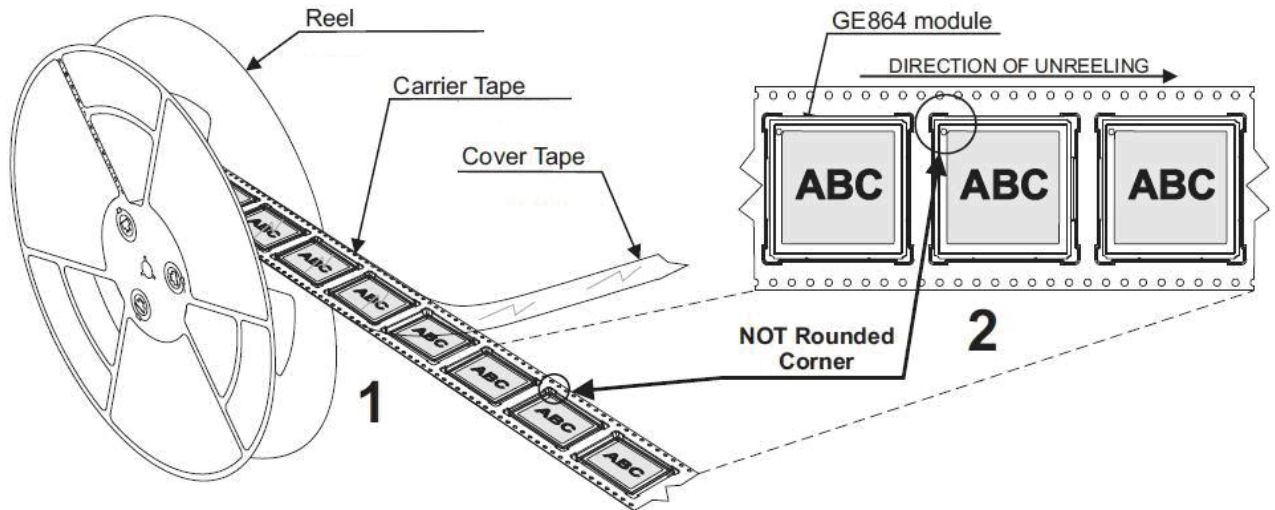
Top view



It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.



Reel Drawing



14.2.1. Moisture Sensibility

The level of moisture sensibility of GE864 module is “3”, in according with standard IPC/JEDEC J-STD-020, take care all the relatives requirements for using this kind of components.



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Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and to have their complete product tested and approved for FCC compliance.



The European Community provides some Directives for the electronic equipments introduced on the market. All the relevant information are available on the European Community website:

<http://europa.eu.int/comm/enterprise/rtte/dir99-5.htm>

The text of the Directive 99/05 regarding telecommunication equipments is available, while the applicable Directives (Low Voltage and EMC) are available at:

http://europa.eu.int/comm/enterprise/electr_equipment/index_en.htm

