Trenz Electronic GmbH
Brendel 20
32257 Bünde, Germany
www.trenz-electronic.de

Spartan-II Development System

2002-September-27

Product Specification TE-XC2S Rev. 01

Overview

The Spartan-II Development System (TE-XC2S) was designed to implement a simple yet powerful platform for FPGA development, which can be easily expanded to reflect your application's requirements. The Development System is built from two distinct concepts: *Base Boards* and *Expansion Boards*.

The Base Board carries an FPGA of a specific family and type and all required circuitry to supply and configure this device. Special care is taken to provide user's access to the device family's feature set. The Base Board is available with two FPGA variants (200k or 500k gates Spartan-II device)

Expansion Boards can be attached to a Base Board to add application specific components. Care has been taken to make Expansion connector fully compatible to previous versions of this board.

Up to four Expansion Boards may be added to a single Base Board, giving plenty of room to your circuit ideas.

The Spartan-II Development System provides the following key features:

- XC2S200 (XC2S50) FPGA with up to 200k (50k) system gates, 56k (32k) bits of block RAM and up to 200MHz clock speed.
- XC18V02 Flash PROM socket and XC17S200A OTP socket, providing non-volatile configuration.
- Access to 137 user I/Os and 4 global clocks.
- On-board voltage regulation. External 8-12V DC Power supply needed.
- Fully compatible to Xilinx' *WebPACK ISE* design software- a complete design entry, simulation, synthesis and implementation environment free of charge.
- Fully compatible to Xilinx' *Parallel Cable III* preventing the need of an additional download cable.

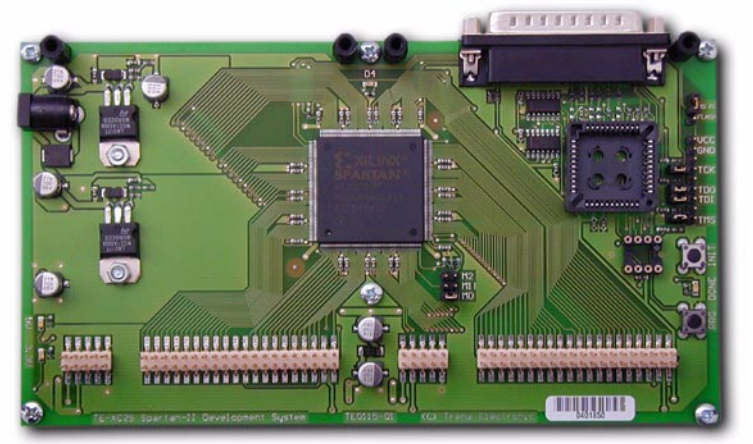

Figure 1: Spartan-II Development System (HW Revision 01)

Base Board

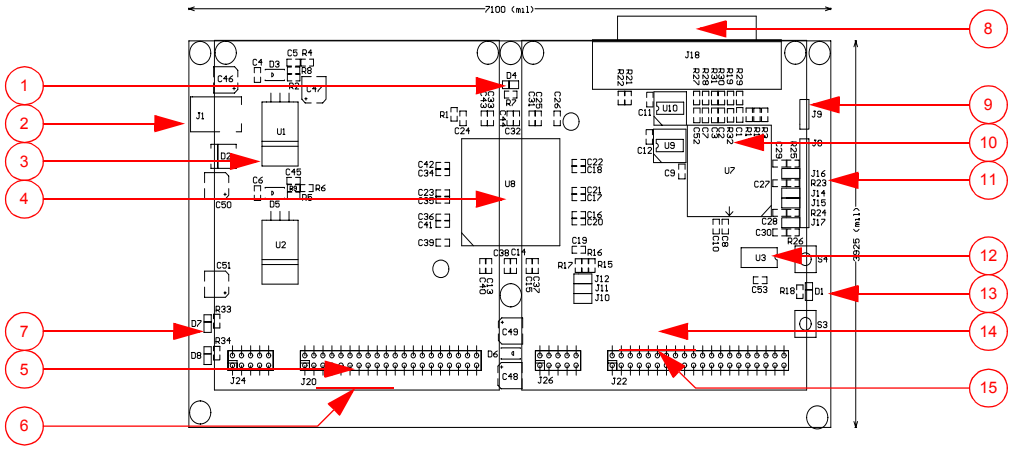

Figure 2: Spartan-II Base Board

1. User LED D4
2. Power Supply Connector
3. Voltage Regulators
4. XC2S200 (XC2S50) FPGA
5. Expansion Connector #1
6. Expansion Connector #2 (solder side)
7. Power LEDs
8. Parallel Port Connector
9. Flash select Jumper J8
10. XC18V02PC44C Flash PROM socket
11. JTAG connector and Jumpers J14-J17
12. XC17S200A OTP socket
13. “DONE” LED and Push Buttons S3 and S4
14. Expansion Connector #3
15. Expansion Connector #4 (solder side)

Configuration Section

Figure 3 shows the configuration section of the schematics. Refer to *Figure 2* to locate the components.

The FPGA configuration is loaded from:

- PC via parallel download cable
- on-board, socket mount Flash PROM (XC18V02, reprogrammable via PC)
- on-board, socket mount OTP PROM (XC17S200A)

The board, by default, is delivered with sockets only. You may insert the appropriate devices needed.

Set J9, according to the presence of on-board boot devices. See Table 1 for Jumper settings.

Jumper	Flash/OTP	no Flash/OTP (default)
J9	1-2	2-3

Table 1: Flash / OTP select

Spartan-II FPGA is either configured from the XC18V02 Flash PROM, or the XC17S200A OTP in *Master Serial Mode*, or via JTAG in *Boundary-Scan Mode*. The configuration mode is selected by setting J10, J11 and J12 (M0, M1, M2) accordingly. Default is JTAG.

D1 (DONE) lights up, once the FPGA is configured.

FPGA configuration can be triggered any time by pressing push button S3 (PRG).

Configuration may be delayed by pressing push button S4 (INIT), this button may be used as a user i/o after configuration, e.g. to function as a reset button.

Programming of the Flash PROM or configuration of the FPGA is performed using the Xilinx *PROM File Formatter* and *JTAG Programmer* software.

Jumper	Master Serial	Boundary-Scan (default)
J10 / M0	open	closed
J11 / M1	open	open
J12 / M2	open	open

Table 2: Configuration Jumpers

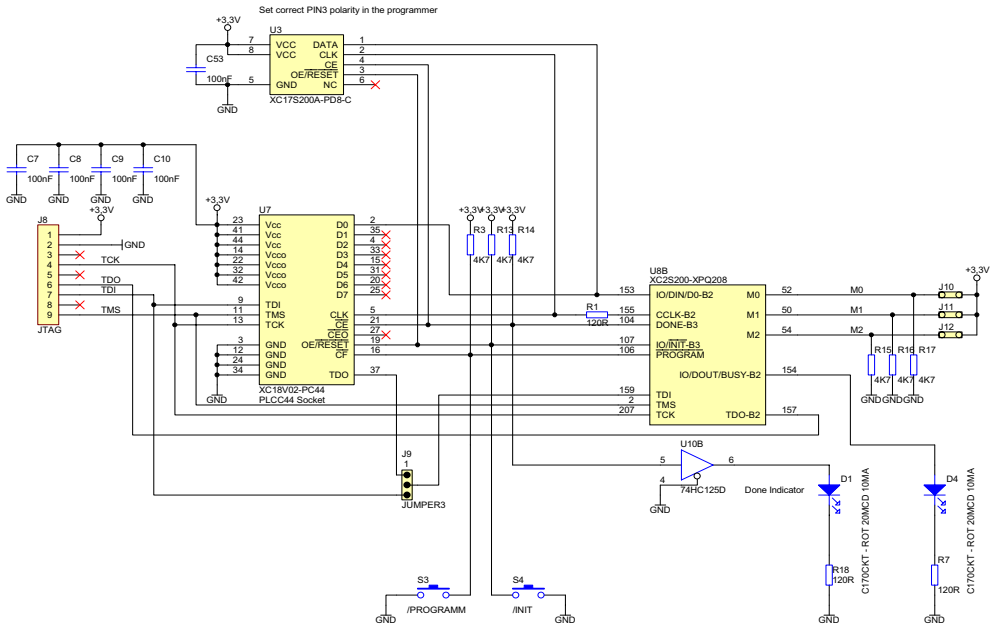

Figure 3: Configuration Section

Download Cable

Figure 4 shows the download cable schematics. Refer to *Figure 2* to locate the components.

The download functionality is 100% compatible to Xilinx' *Parallel Cable III*. This circuitry may be used for PROM programming, FPGA configuration and readback via JTAG.

The download functionality may be detached from the JTAG chain by removing J14, J15, J16, and J17 (TDO, TDI, TCK, TMS). This is useful in case other download cables, e.g. the Xilinx *MultiLINX* cable, are used. These cables may be attached to J8.

Signal	Parallel Cable (default)	Other Cable
J14	closed	open
J15	closed	open
J16	closed	open
J17	closed	open
J8	no connect	JTAG leads

Table 3: Download Jumpers

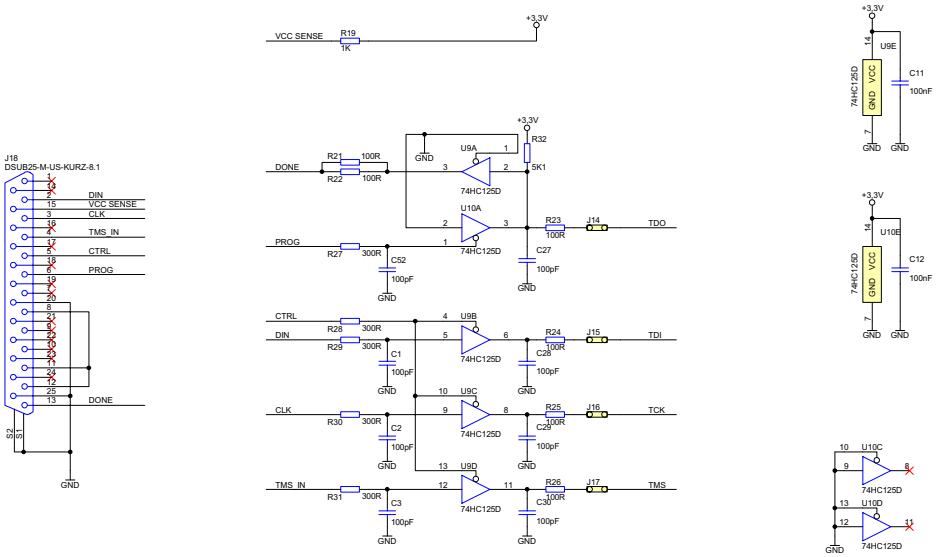

Figure 4: Download Cable

Power Supply

Figure 5 shows the power supply schematics. Refer to *Figure 2* to locate the components.

The input DC power (8 to 12 Volts) may be provided by an plug-in wall adaptor. Current rating depends on the Design loaded into the FPGA, and external circuits connected to the expansion connectors. A base board with one Buttons and Lights, configured with the Buttons and Lights Demo draws about 110mA.

LEDs D3 and D4 signal presence of the 5V and 3.3V supply voltages.

All Vcco pins are attached to 3.3V. This results in global use of the LVTTL standard for all I/O pins.

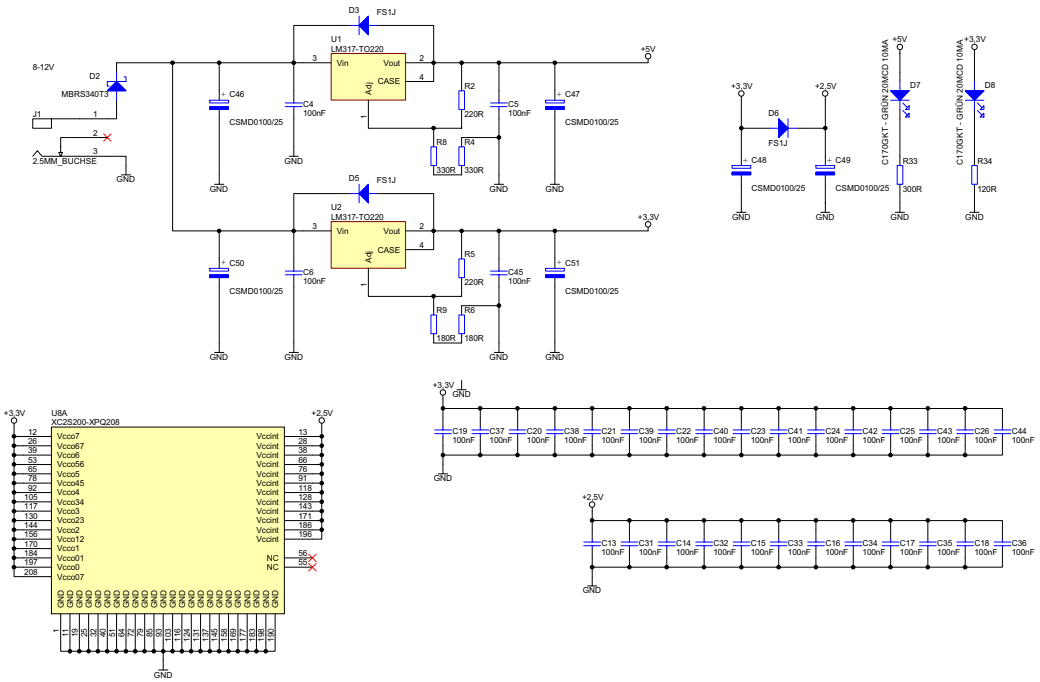

Figure 5: Power Supply

Expansion Connectors

The board provides four Expansion Connectors, which may be used to connect up to four optional Expansion Boards to a single Base Board.

The I/Os of Spartan-II FPGAs are organized in 8 banks. Two adjacent banks form a quadrant. See *Figure 6* for further details. Each of the four Expansion Board Connectors carries the I/O and GCLK lines of one specific FPGA quadrant:

- *Expansion Connector #1:* Banks 0 and 7
- *Expansion Connector #2:* Banks 1 and 2
- *Expansion Connector #3:* Banks 3 and 4
- *Expansion Connector #4:* Banks 5 and 6

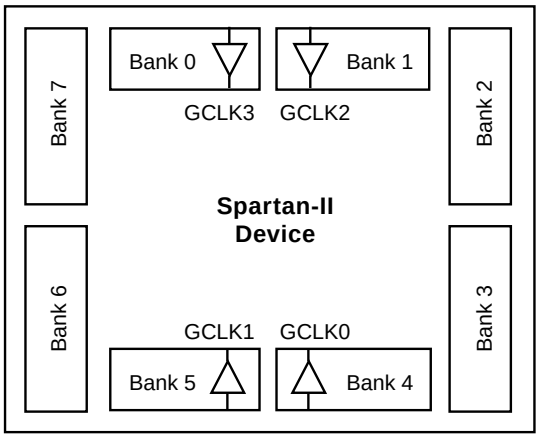

Figure 6: I/O Banking

Dual purpose pins are consequently not used on the Expansion Connectors, resulting in the highest possible flexibility for expansion circuitry design.

Every Expansion Connector carries:

- 1 clock input
- 33 - 35 I/Os organized in two banks

For the complete board, this sums up to:

- 4 global clocks
- 137 user I/Os

In addition to the I/O and clock lines, each of the four Expansion Board Connectors is accompanied by an Expansion Power Connector providing 3.3V and 5V to the Expansion Boards

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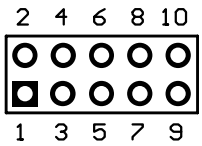

Figure 7: Expanion Power (top view)

See *Figure 2* for Pin 1 marking.

Pin	Signal
1	+3,3V
2	+3,3V
3	+5V
4	+5V
5	nc
6	nc
7	nc
8	nc
9	GND
10	GND

Table 4: Expansion Power

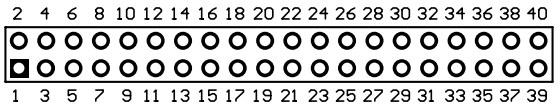

Figure 8: Expansion Connector (top view)

Table 5 summarizes the pin mapping of the Expansion Board Connectors.

Pin	Name	FPGA Pin on Expansion Connector				Old name (TE0115-00)
		#1 (J20)	#2 (J21)	#3 (J22)	#4 (J23)	
1	CLK	185	182	80	77	CLK_A1
2	IO1	187	181	81	75	CLK_A2
3	IO2	188	180	82	74	CLK_A3
4	IO3	189	179	83	73	CLK_A4
5	IO4	191	178	84	71	IOP_A1
6	IO5	192	176	86	70	ION_A1
7	IO6	193	175	87	69	IOP_A2
8	IO7	194	174	88	68	ION_A2
9	IO8	195	173	89	67	IOP_A3
10	IO9	199	172	90	63	ION_A3
11	IO10	200	168	94	62	IOP_A4
12	IO11	201	167	95	61	ION_A4
13	IO12	202	166	96	60	IOP_A5
14	IO13	203	165	97	59	ION_A5
15	IO14	204	164	98	58	IOP_A6
16	IO15	205	163	99	57	ION_A6
17	IO16	206	162	100	49	IOP_A7
18	IO17	3	161	101	48	ION_A7
19	N.C	N.C.	N.C.	N.C.	N.C.	Vcco_A
20	N.C.	N.C.	N.C.	N.C.	N.C.	Vref_A
21	EXTRA1	22	160	102	N.C.	-
22	EXTRA2	N.C.	134	126	N.C.	-
23	IO18	4	152	108	47	IOP_B1
24	IO19	5	151	109	46	ION_B1
25	IO20	6	150	110	45	IOP_B2
26	IO21	7	149	111	44	ION_B2
27	IO22	8	148	112	43	IOP_B3
28	IO23	9	147	113	42	ION_B3
29	IO24	10	146	114	41	IOP_B4
30	IO25	14	142	115	37	ION_B4
31	IO26	15	141	119	36	IOP_B5
32	IO27	16	140	120	35	ION_B5
33	IO28	17	139	121	34	IOP_B6
34	IO29	18	138	122	33	ION_B6
35	IO30	20	136	123	31	IOP_B7
36	IO31	21	135	125	30	ION_B7
37	N.C.	N.C.	N.C.	N.C.	N.C.	Vcco_B
38	N.C.	N.C.	N.C.	N.C.	N.C.	Vref_B
39	EXTRA3	23	133	127	29	-
40	EXTRA4	24	132	129	27	-

Table 5: Expansion Connector Pins

Signals Vcco, Vref, VRP_A, VRN_A, VRP_B, VRN_B are not connected in TE0115-00 and are removed in TE0115-01.

In order to use TE-XC2S we recommend the following equipment:

- Product accompanying CD-ROM
- PC with accompanying parallel download cable
- Plug-in wall adaptor (8-12Volts DC, >= 500mA)

Hardware Revision

All expansion boards designed for Revision 00 can unaltered be used in Revision 01.

The HW revision 01 differs from 00 by the following items:

- Second (smaller) FPGA option
- On-board voltage regulation replace ATX connector
- Sockets for OTP and Flash PROMs
- More IOs routed to the expansion connectors

Product Configuration Options

The TE-XC2S is available in two configuration options. Please refer to the Xilinx Spartam-II Product Specification for details.

Order No.	Spartan-II Device
TE0115-01	XC2S200
TE0115-01L	XC2S50

Table 6: Product Configuration Options

References

- *Spartan-II 2.5V FPGA Family Product Specification*
  Xilinx, Inc.
  October 31, 2000
- *XC18V00 Series of In-System Programmable Configuration PROMs Product Specification*
  Xilinx, Inc.
  April 4, 2000
- *Spartan-II FPGA Family Configuration and Readback*
  XAPP176
  Xilinx, Inc.
  December 4, 1999
- *Configuration and Readback of Virtex FPGAs Using (JTAG) Boundary-Scan*
  XAPP139
  Xilinx, Inc.
  February 18, 2000
- *JTAG/ Parallel Download Cable Drawing*
  Xilinx, Inc.
  July 10, 1996
- *HW-JTAG-PC Cable Contents*
  Xilinx, Inc.
- *Hardware Book*
  http://www.hardwarebook.net/
  June 08, 2001

Revisions History

Version	Date	Who	Description
0.9	2001jul31	FB	Created
1.0	2001sep12	FB	Minor HW changes
1.1	2002jul23	TT	New HW revision

Table 7: Revisions History