Overview

The Retrocomputing Baseboard carries the Spartan-3 Micromodule, and extends it with various interfaces, display options and memory expansions to form a fully-featured System-On-Chip development platform.

Retrocomputing deals with emulation of former workstations, home computers and game consoles of the 80s, and is pushed by numerous projects around the web. The Retrocomputing Baseboard in combination with the Spartan-3 Micromodule is tailored to FPGA-based emulation of game consoles and home computers.

JTAG connection for compatibility with Xilinx parallel cable III and IV, as well as with the low cost Trenz Electronic JTAG Programmer are available.

Flexible power supply via USB, or a dedicated DC jack is possible.

- Illuminated LCD-Display with 2x16 Characters
- 256k x 16Bit Static RAM
- 512k x 16Bit Flash Memory
- Compact-Flash Slot (Type I)
- RS232-Interface Port
- USB Port
- Two PS2 Ports e.g. for connecting a keyboard and/or mouse
- Stereo Audio in/out via 3.5mm stereo jack
- VGA monitor output (512 colors)
- 9-pin game port connector for standard C64 joystick
- Onboard control buttons (5x)
- Standard infrared receiver
- 4 user LED's
- 4 user jumper
- All signals available on header w. 2.54mm (100mil) pitch
- Board supply via DC jack or USB JTAG header compatible to TE JTAG Programmer, Xilinx parallel cable III and IV

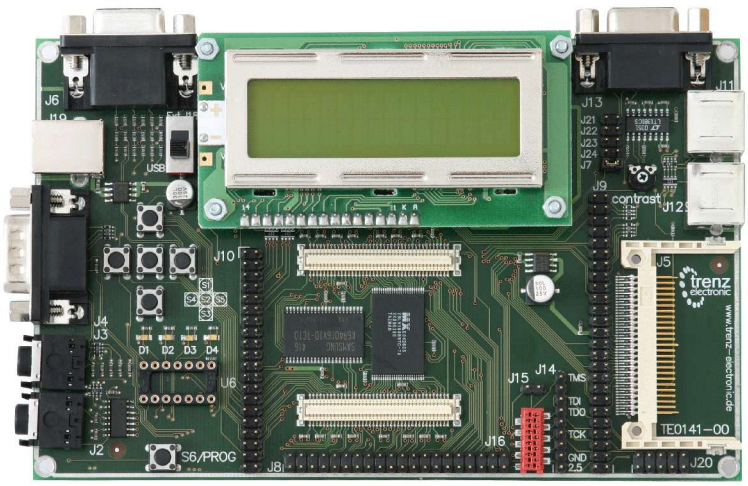

Figure 1: Baseboard without Micromodule

Features

Details

Baseboard configuration

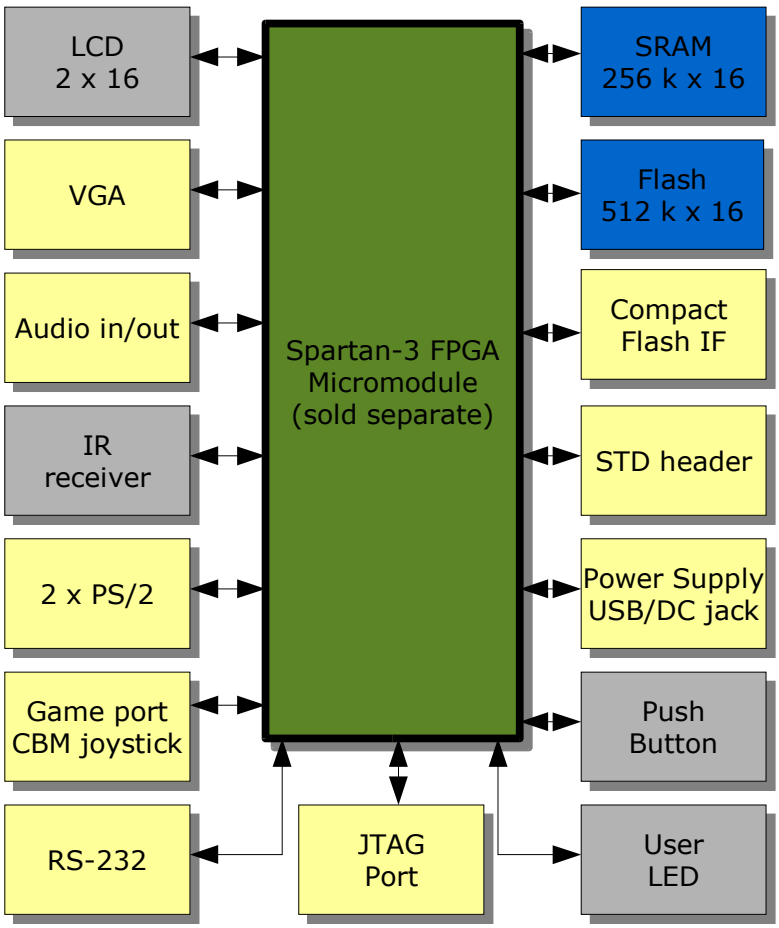

Figure 2: Baseboard block diagram

To locate the jumper and connectors see Figure 3.

Power Supply

There are two power supply options on the board.

5V-DC powered

Set the sliding switch J18 to EXT, and connect a 5V DC supply to the DC-Jack (J17).

USB powered

Set the sliding switch J18 to USB, and connect a standard USB cable. In this case there is a current limiting power switch in the path. Total current is limited to 700mA max.

Header Power Pins

Power pins on the IO headers can be used to supply external circuits. For details see Figure 4.

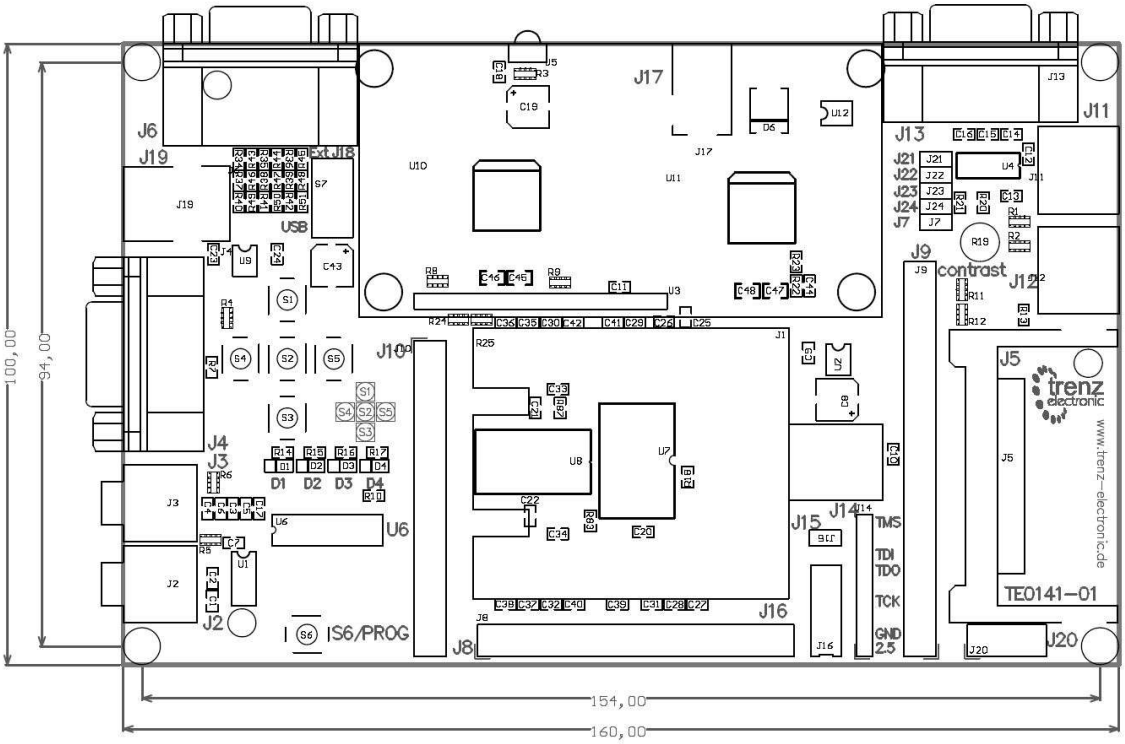

Figure 3: Place plan (Dimensions in mm)

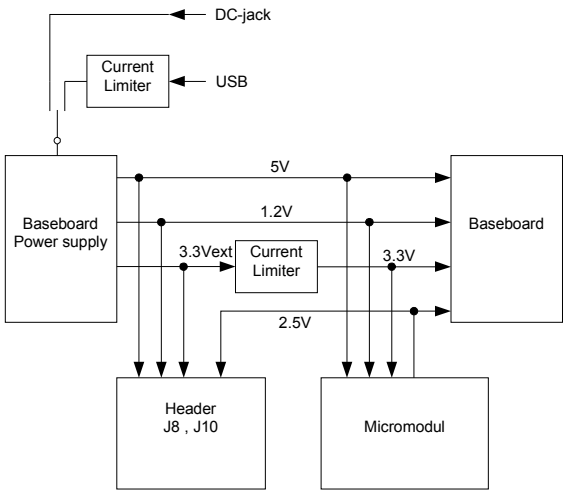

Figure 4: Power supply block diagram

The baseboard generates 3.3V and 1.2V, and the micromodule produces 2.5V.

The 1.2V of the baseboard is used to power the FPGA core externally, therefore the EXT 1.2V EN Pin of the micromodule is set low.

There is a current limiter added in the 3.3V path. This is necessary to meet the VCCIO ramp-up time needed by the FPGA.

For external use the 3.3V pins on header J8 and J10 are directly connected to the voltage regulator without current limiting.

Power Supply for FPGA IO

VCCIO for bank's 2,3,6 and 7 is connected to 3.3V.

Warning: Spartan-3 IOs are not 5V tolerant. Applying 5V to any pin, may cause damage to the FPGA.

Clock supply

To add another crystal oscillator there is a 14-pin socket (U6), which is compatible to a 8-pin and 14-pin oscillator module. You have to attach it left-justified to the socket.

Pin	Signal
1	N.C.
4, 7	GND
8, 11	GCLK0_4
14	+5V

Table 1: Oscillator socket

JTAG Programming

There are two JTAG connectors available. J14 supports the older 9 pin Xilinx header. Table 2 shows it's pin assignments.

Pin	Signal
1	VREF
2	GND
3	N.C.
4	TCK
5	N.C.
6	TDO
7	TDI
8	N.C.
9	TMS

Table 2: 9 Pin JTAG Connector

For ease of use with the Trenz Electronic JTAG Programmer, a 10 pin header (J20) has been added. By using it, the board supplies the JTAG Programmer with power over an additional voltage line (pin 7).

Pin	Signal
1	GND
2	MODE
3	VREF
4	TCK
5	GND
6	TMS
7	VCC
8	TDI
9	GND
10	TDO

Table 3: 10 Pin JTAG Connector

During programming, jumper J15 can be bridged to switch the FPGA to JTAG only mode. If you use the 10 pin header with Trenz Electronic JTAG Programmer, the connection is made on the programmer by default. (see Table 3, pin 2.)

Please note that the Micromodule won't configure from Flash if the jumper is set, or if the Trenz Electronic JTAG Programmer is connected.

Pushbutton S6/Prog

The pushbutton S6 is connected to the prog line on module revision 01 (TE0140-01) and above. By pressing the button, the FPGA configuration will be reloaded from Flash. It has no function, when used with module Revision 00 (TE0140-00).

Note: Module Revisions TE0140-01 and up are labeled appropriately, Revision TE0140-00 is labeled Rev. 0.1.

Memory Subsystem

The memory subsystem consist of a 16-Bit data bus, and a 20-Bit address bus with the following devices attached:

- Static RAM
- Flash memory
- Compact Flash (Type I) slot

SRAM

An asynchronous Static RAM of type IDT71V416S or similar is attached to the memory bus to store volatile data. E.g. a processor system's stack and heap data.

The RAM is fast enough to serve as zero-waitstate main memory for typical processing applications. Consult the RAM's data sheet for timing diagrams. These signals belongs to the RAM control:

Signal	Function
/R_CS	Chip select
/WE	Write enable
/R_OE	Output enable
/R_BLE	Lower byte enable
/R_BHE	Higher byte enable

Table 4: RAM Control Signals

FLASH memory

A AMD flash memory of type AM29LV800B or similar, with 8Mbits of storage (512Kx16) is attached to the memory bus, to store non-volatile data.

Signal	Function
/FL_CS	Chip select
/WE	Write enable
/FL_OE	Output enable
/FL_BYTE	Byte/Word mode
/FL_BY	Output busy

Table 5: Flash Control Signals

Compact Flash slot

For flexible use and easy data storage a Compact Flash (CF Type I) slot is added to the memory bus, compatible with all available Type I CF-Cards. A current limiter cares for a failure-free and switchable power supply. Apart from the memory bus, the following signals exist:

Signal	Function	Direc. (FPGA)
/CF_PWR_EN	Power Enable	OUT
CF_/WE	Write Enable	OUT
CF_/REG	Memory select	OUT
CF_/CS0	Mode	OUT
CF_/CS1	Mode	OUT
CF_/RESET	Reset	OUT
CF_/IRQ	Busy,IRT Request	IN
CF_/IORD	Read strobe	OUT
CF_/IOWR	Write strobe	OUT
CF_/WAIT	Wait,IOReady	IN
CF_/DASP	DASP,SPKR,BVD2	I/O
CF_/PDIAG	PDIAG,STSCHG,BVD1	I/O
CF_/CD1	Card Detect	IN
CF_/CD2	Card Detect	IN
/IOIS16	Write Protection	IN
CF_/OE	Output Enable	OUT

Table 6: Control Signals

The function of these signals depends on the internal Mode of the CF-Card. For more details see the CF specification.

All available signals on the CF-Slot are also presented on the J9 header.

LCD-Display

A Polytronix liquid crystal display of type PC-160203 with 2x16 characters is attached to provide a convenient way of visualizing textural data.

You can adjust the contrast by the potentiometer. The background lighting is enabled by the jumper J7.

It works in 4-Bit mode and has the following signals:

- LCD_D4
- LCD_D5
- LCD_D6
- LCD_D7
- LCD_R/W
- LCD_E
- LCD_RS

When initiating the LCD you have to set it into 4-Bit mode by sending a '02h' command. Then the higher nibble is sent first, and the lower nibble is sent second when writing other commands or 8 Bit data into the LCD RAM. For more details see the lcd module in the example project and the lcd datasheet.

USB Connector

The data lines are directly connected to the USB interface chip on the Micromodule.

RS232 Interface

J13 is a standard 9-pin DSUB connector. There is an interface driver chip in the path, so you can directly connect a RS232-compliant device like a PC.

The signal naming in Table 7, and the signals available in the FPGA are seen from the external interface.

Pin	Signal
1	N.C.
2	RxD (serial out)
3	TxD (serial in)
4	N.C.
5	GND
6	N.C.
7	RTS (in)
8	CTS (out)
9	N.C.

Table 7: DSUB-9 Connector

The following signals are connected to the FPGA:

- FPGA_TxD (from pin 3 J13, input)
- FPGA_RxD (from pin 2 J13, output)
- FPGA_RTS (from pin 7 J13, input)
- FPGA_CTS (from pin 8 J13, output)

PS/2 Connector

There are two Mini DIN6 Jacks, J11 and J12, for connecting PS/2 devices like a keyboard or mouse. When using them, the user jumpers J21 to J24 have to be removed, because both share the signals to the FPGA (see the jumper paragraph).

Pin	Signal
1	PS2_DATA1/2
2	N.C.
3	GND
4	+5V
5	N.C.
6	PS2_CLK1/2

Table 8: Mini DIN6 Connector

The signals Data1 and CLK1 are connected to J11, Data2 and CLK2 to J12.

In the example project, there is a module for reading keyboard commands, called 'ps2'. If you want to add some commands, you will need to edit this section by adding the appropriate SCAN-Code and signal.

Jumper

If you don't need the PS/2 connectors you can use these signals for jumpers.

The signals are pulled up and will be set to ground by the jumper.

Jumper	Signal
J21	PS2_DATA1
J22	PS2_CLK1
J23	PS2_DATA2
J24	PS2_CLK2

Table 9: Jumper J21 to J24

Game Port

On the 9-pin DSUB connector J4 you can plug in a standard C64 Joystick with the following pin assignment.

Button	Signal
1	JOY UP
2	JOY DOWN
3	JOY LEFT
4	JOY RIGHT
5	JOY POT Y
6	JOY FIRE
7	+3.3V
8	GND
9	JOY POT X

Table 10: Game Port Connector

Joy Pot X/Y are the potentiometer output lines. A RC-element is connected to them and the signals Pot X/Y passes to the FPGA. To digitize the resistor value you can use a technique like the single-slope A/D conversion method. The FPGA input acts as the comparator, and to reset the capacitor.

Set the signal line to '0' so the capacitor discharges. Then you set it to tristate and start a timer. The capacitor will charge over the potentiometer of the joystick and a guard resistor. When the signal arrives at '1' you stop counting. The time value is proportional to the resistor value and also to the position of the joystick.

The other signals are pulled-up and directly connected to both the FPGA and the pushbuttons S1 through S5.

For RC time-constant calculations you will need these values:

- R=3k3
- C=22nF

Pushbuttons S1 to S5

These buttons are connected to the game port signals. These signals are pulled-up and will be set to ground by pushing S1 through S5. Table 11 shows the allocations.

Button	Signal
S1	JOY UP
S2	JOY FIRE
S3	JOY DOWN
S4	JOY LEFT
S5	JOY RIGHT

Table 11: Pushbuttons

Audio In & Out

The audio out pins from the FPGA are connected to RC-elements, which have a time constant of 15µs. So you can use digital pulse-width-modulated signals on Aud_Out1/2 to output an analog voltage to the J3 stereo-jack.

The same applies for Aud_Out3/4, too. But they are provided as reference voltage for the Sigma-Delta A/D conversion of the Audio Input jack J2. Therefore you have to implement the converter in the FPGA.

The analog input lines are linked with the positive input of the comparators, and the reference voltage to the negative input. Comp1/2 is the output of the comparator.

The following list summarizes the audio

signals:

- Output (J3)
  - AUD_OUT1
  - AUD_OUT2
- Input (J2)
  - AUD_OUT3
  - AUD_OUT4
  - COMP1
  - COMP2

VGA Monitor Interface

The baseboard provides circuitry to interface with industry-standard VGA monitors. For video output, RGB tuples along with horizontal and vertical sync pulses need to be generated by the FPGA. With the help of an R2R resistor network the three 3-Bit color signals are converted to analog levels. These signals are:

- red
  - FPGA_R0
  - FPGA_R1
  - FPGA_R2
- green
  - FPGA_G0
  - FPGA_G1
  - FPGA_G2
- blue
  - FPGA_B0
  - FPGA_B1
  - FPGA_B2

So you can display 512 colors overall. The synchronisation lines are:

- /HSYNC
- /VSYNC

Infrared Receiver

This is a standard IR Receiver for a carrier frequency of 36kHz, which is used by most transmitters. IR_Data is the signal line passes to the FPGA.

User LED's

D1 to D4 are red LED's for free use. For activating them you have to set the outgoing signal to low.

Pin (J8)	Signal	FPGA	Direc. (FPGA)
1	+5V		
2	+3.3V		
3	+2.5V		
4	+1.2V		
5	GCLK0 4	T9	IN
6	GCLK1 4	R9	IN
7	JOY FIRE	T14	IN
8	JOY RIGHT	R13	IN
9	PS2 DATA2	C3	IN
10	JOY DOWN	P15	IN
11	PS2 CLK2	B1	IN
12	JOY UP	P14	IN
13	LED3	T12	OUT
14	LED4	R11	OUT
15	LED2	R12	OUT
16	R16	R16	I/O
17	POT Y	G12	IN
18	POT X	G13	IN
19	COMP2	F12	IN
20	COMP1	F13	IN
21	AUD OUT4	D12	OUT
22	AUD OUT3	D11	OUT
23	AUD OUT2	E10	OUT
24	AUD OUT1	D10	OUT
25	LED1	T13	OUT
26	A20	G3	OUT
27	/R OE	K16	OUT
28	A19	H3	OUT
29	A18	H4	OUT
30	/CF PWR EN	P2	OUT
31	A13	E2	OUT
32	A17	B16	OUT
33	A12	E1	OUT
34	A16	D2	OUT
35	A11	F3	OUT
36	A15	D1	OUT
37	/WE	G1	OUT
38	A14	E3	OUT
39	GND		
40	GND		

Table 12: J8 Connector

Pin (J10)	Signal	FPGA	Direc. (FPGA)
1	+5V		
2	+3.3V		
3	+2.5V		
4	+1.2V		
5	LCD D7	M1	I/O
6	LCD D6	L4	I/O
7	LCD D5	L5	I/O
8	LCD D4	N1	I/O
9	LCD E	N2	OUT
10	LCD R/W	N3	OUT
11	LCD RS	P1	OUT
12	P8	P8	I/O
13	/VSYNC	R1	OUT
14	N8	N8	I/O
15	/HSYNC	J13	OUT
16	T8	T8	I/O
17	P7	P7	I/O
18	R6	R6	I/O
19	P6	P6	I/O
20	IR DATA	D3	IN
21	R5	R5	I/O
22	PS2 DATA1	C2	IN
23	P5	P5	I/O
24	PS2 CLK1	C1	IN
25	FPGA B2	M14	OUT
26	FPGA B1	M15	OUT
27	FPGA B0	M16	OUT
28	FPGA G2	L13	OUT
29	FPGA G1	M13	OUT
30	FPGA G0	N16	OUT
31	FPGA R2	N15	OUT
32	FPGA CTS	E11	OUT
33	FPGA R1	N14	I7O
34	FPGA RxD	J14	OUT
35	FPGA R0	P16	I/O
36	FPGA RTS	K12	IN
37	JOY LEFT	K13	IN
38	FPGA TxD	L12	IN
39	GND		
40	GND		

Table 13: J10 Connector

Pin (J9)	Signal	FPGA	Direc. (FPGA)
1	GND		
2	CF /CD1	K5	IN
3	D3	G14	I/O
4	D11	F15	I/O
5	D4	F14	I/O
6	D12	E16	I/O
7	D5	E15	I/O
8	D13	E14	I/O
9	D6	D16	I/O
10	D14	D15	I/O
11	D7	E13	I/O
12	D15	C16	I/O
13	CF /CS0	D7	OUT
14	CF /CS1	D5	OUT
15	A10	F2	OUT
16	N.C.		
17	CF /OE	M4	OUT
18	CF /IORD	F4	OUT
19	A9	G4	OUT
20	CF /IOWR	F5	OUT
21	A8	J1	OUT
22	CF /WE	D8	OUT
23	A7	J2	OUT
24	CF /IRQ	E4	IN
25	CF VCC		
26	CF VCC		
27	A6	K2	OUT
28	GND		
29	A5	K1	OUT
30	N.C.		
31	A4	L3	OUT
32	CF /RESET	E6	OUT
33	A3	L2	OUT
34	CF /WAIT	E7	IN
35	A2	M3	OUT
36	N.C.		
37	A1	K15	OUT
38	CF /REG	G5	OUT
39	A0	D14	OUT
40	CF /DASP	J4	I/O
41	D0	H15	I/O
42	CF /PDIAG	J3	I/O
43	D1	H14	I/O
44	D8	H16	I/O
45	D2	G16	I/O
46	D9	H13	I/O
47	/IOIS16	K3	IN
48	D10	G15	I/O
49	CF /CD2	K4	IN
50	GND		

Table 14: J10 Connector

Ordering Details

Package contents

- Carrier Board
- Documentation CD-ROM including schematics

Order number

The order number is: TE0141-01

History

Rev.	Date	Who	Description
0.9	20041020	TS	Created
0.91	20050315	TT	CF Type I added

Table 15: History