Overview

This small, but powerful Altera FPGA platform is designed for SoC (System-On-Chip) solutions. To ensure maximum flexibility, two banks of SRAM, conventional Flash and a large NAND-Flash are integrated on-board.

Combined with peripherals like clock oscillator, watchdog and RS-232 serial port, the Cyclone Micromodule is fully compatible to the JOPcore (Java-Optimized-Processor) HDL design and forms a powerful Java platform for your application.

As a small-sized module, it can be combined with our ready-to-use base boards, or as a design-in of a complete Java processor system.

Features

- Altera Cyclone EP1C6Q240 or EP1C12Q240 FPGA
- 512 KByte FLASH (for FPGA configuration and program code)
- 1 MByte fast SRAM (2 x 256K x 16)
- 32 MByte NAND FLASH
- ByteBlasterMV port
- Watchdog with LED
- EPM7064 PLD (loads FPGA config from FLASH on watchdog reset)
- Voltage regulator (1.5 V output)
- 20 MHz Quartz oscillator (up to 640 MHz internal clock generated by PLL)
- RS-232 serial interface (MAX3232)
- 56 general purpose IO pins
- Small board size (60mm x 48mm)

Figure 1: Cyclone Module (component side)

Details

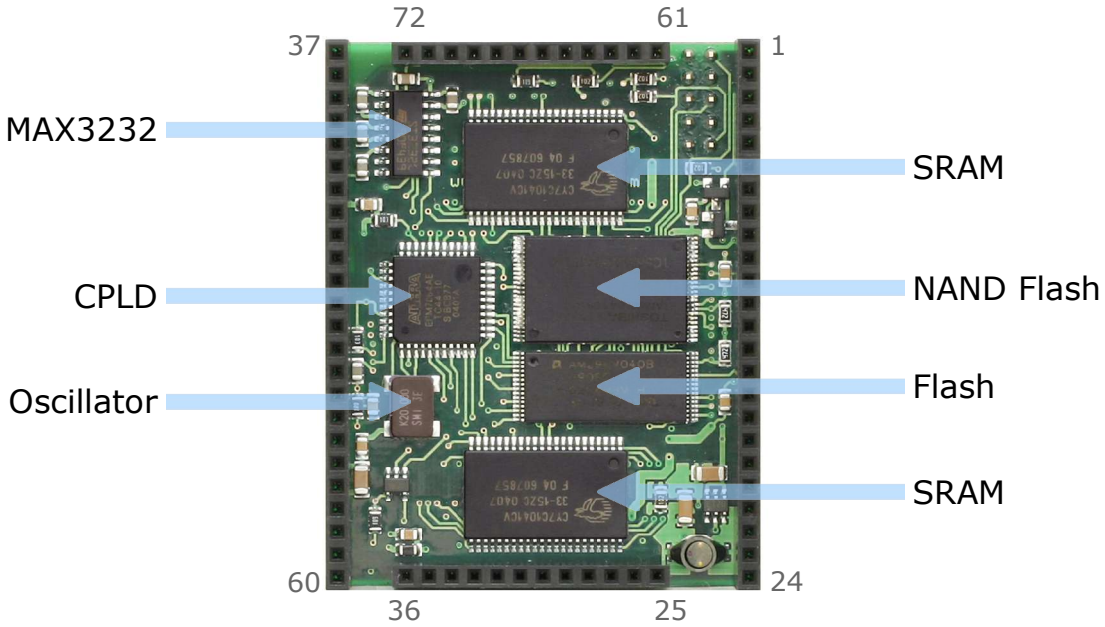

Figure 2: Cyclone Module (solder side)

Power Supply

A regulated 3.3V supply on pin 1 and 2 of connector JM1 is necessary to supply power to the board. Polarity and magnitude of the power source must be carefully adjusted when connected to the board.

Note: Wrong power supply to the 3.3 Volt inputs may cause damage to the module!

An on-board voltage regulator generates the 1.5 V FPGA core supply.

Clock supply

A 20MHz clock signal is available produced by a crystal clock oscillator. The Cyclone FPGA is featured with two programmable PLLs which can generate output frequencies of up to 640MHz.

Generation of a PLL model is eased by a configuration wizard incorporated in Altera's Quartus design software. Open the MegaWizard Plug-in Manager in menu 'Tools', choose appropriate PLL and type in the parameter dialog.

Memory Subsystem

The memory hierarchy consists of:

- Two 512kB SRAMs (A & B) (CY7C1041CV, Cypress Semiconductors)
- 512kB conventional Flash (AM29LV, AMD)
- 32MB NAND Flash (TC58DVM82AF1FT, Toshiba)

In order to gain maximum bandwidth and reduce reflections, minimal trace lengths are used between FPGA and the SRAM.

Table 1 provides an overview of the different address bus and data path sized to the memory subsystem.

	Addressbus	Databus
SRAM A/B	A0 - A17	D0 - D15
Flash	A0 - A18	D0 - D7
NAND-Flash	A0: CLE A1: ALE	D0 - D7

Table 1:Bus System

There are different control lines for each component, so that is possible to implement two independent CPUs. Both Flash memories share the same write and read enable signals.

	Control Signals	Pin
SRAM A	RAMA_NCS	78
	RAMA_NOE	73
	RAMA_NWE	105
	RAMA_NLB	77
	RAMA_NUB	75
SRAM B	RAMB_NCS	223
	RAMB_NOE	228
	RAMB_NWE	196
	RAMB_NLB	224
	RAMB_NUB	226
Flash	FL_NCS	37
	FL_NOE	24
	FL_NWE	15
NAND-Flash	FL_NCS2	23
	FL_RDY	29
	FL_NOE	24
	FL_NWE	15

Table 2: Control Lines

Serial Interface

A MAX3232 transceiver is added for RS-232 compliant COM interface. The following signals are provided on the FPGA.

Signal	Pin	Dir. (FPGA)
SER_TXD	178	OUT
SER_NRTS	177	OUT
SER_RXD	153	IN
SER_NCTS	28	IN

Table 3: RS-232 Signals

Watchdog

Because this board is developed for SoC applications, a MAX823 watchdog timer is added. This device is directly connected to the PLD to trigger download of the configuration to the FPGA. The watchdog input and the LED are connected to the signal WD on Pin 166. If this pin remains either high or low for longer than 1.6s, a reset is generated. To disable this function, change the PLD configuration.

ByteBlasterMV port

The CPLD and FPGA are connected to this configuration port. Connect the ByteBlaster to the parallel port of your PC and use the JTAG mode to download the configuration to the device.

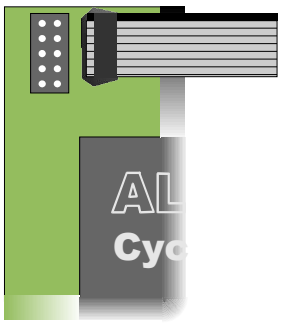

Figure 3: Connecting Programmer

Signal	Pin
TCK	1
GND	2
TDO	3
VCC	4
TMS	5
VCC	6
nc	7
nc	8
TDI	9
GND	10

Table 4: ByteBlaster port

CPLD

To use the Flash for FPGA configuration storage a device is needed to download the data from memory to FPGA. This is done by the CPLD, if it's programmed with the provided file and when a watchdog reset occurs. This file is placed at

...quartus\cycconf\cyc_conf.pof

of the project tree. A dummy file called *cyc_conf_init.pof* exists to retract automatic configuration by reprogramming the CPLD.

FPGA Programming from Flash

To download the FPGA configuration into Flash a program running on JOP that uses the serial interface has to be loaded first. The following steps are necessary:

1. configure the FPGA over ByteBlaster port
2. download a program over serial line
3. download the configuration file over serial line to the Flash
4. configure CPLD for automatic loading

To simplify this procedure unzip the file *program.zip*, copy the *.ttf* file of your design into this directory and execute the batchfile by typing:

program your_design.ttf COM1

Prior to the download, connect the board to the PC with the ByteBlaster and the serial RS-232 interface.

IO's

There are 56 user-defined IOs in addition to the serial lines and the power supply available. See the pin assignment in Table 5 for details. The pins are numbered from top to bottom and from left to right.

To allocate the pin names use the tcl script cypins.tcl in Quartus.

Warning: Cyclone FPGA IOs are not 5V tolerant! Applying 5V to any pin may cause severe damage to the device.

Location	Pin (JM1)	Signal	Pin (FPGA)
Left	1	+3.3V	-
	2	GND	-
	3	IO_L1	2
	4	IO_L2	3
	5	IO_L3	4
	6	IO_L4	5
	7	IO_L5	6
	8	IO_L6	7
	9	IO_L7	8
	10	IO_L8	11
	11	IO_L9	12
	12	IO_L10	13
	13	GND	-
	14	IO_L11	38
	15	IO_L12	39
	16	IO_L13	41
	17	IO_L14	42
	18	IO_L15	43
	19	IO_L16	53
	20	IO_L17	54
	21	IO_L18	55
	22	IO_L19	56
	23	IO_L20	57
	24	GND	-
Bottom	25	IO_B1	58
	26	IO_B2	59
	27	IO_B3	60
	28	GND	-
	29	IO_B4	61
	30	IO_B5	62
	31	IO_B6	120
	32	IO_B7	121

Location	Pin (JM1)	Signal	Pin (FPGA)
Bottom	33	GND	-
	34	IO_B8	122
	35	IO_B9	123
	36	IO_B10	124
Right	37	GND	-
	38	IO_R1	176
	39	IO_R2	175
	40	IO_R3	174
	41	IO_R4	173
	42	IO_R5	170
	43	IO_R6	169
	44	GND	-
	45	IO_R7	168
	46	IO_R8	167
	47	IO_R9	163
	48	IO_R10	162
	49	IO_R11	161
	50	IO_R12	160
	51	IO_R13	159
	52	GND	-
	53	IO_R14	140
	54	IO_R15	138
	55	IO_R16	136
	56	IO_R17	134
	57	IO_R18	132
	58	IO_R19	128
	59	IO_R20	126
	60	GND	-
Top	61	IO_T1	1
	62	IO_T2	240
	63	IO_T3	239
	64	GND	-
	65	IO_T4	181
	66	IO_T5	180
	67	IO_T6	179
Top	68	TXD (OUT)	-
	69	NRTS (OUT)	-
	70	RXD (IN)	-
	71	NCTS (IN)	-
	72	GND	-

Table 5: Pin assignment

Ordering Details

Package contents

- Cyclone Board
- Documentation CD-ROM

Order number

The order number is: TE0180-00

History

Rev.	Date	Who	Description
0.9	2004-12-15	TS	Created
1.0	2005-01-22	FST	Revised

Table 6: History