Trenz Electronic GmbH

info@trenz-electronic.de
www.trenz-electronic.de

BaseIO for Cyclone Board

Rev. 1.0 as of 2005-01-22

User's Manual

Overview

BaseIO is an IO extension carrier board design for the Cyclone FPGA board. The peripherals are compatible to the JOPcore HDL implementation, a Java-optimized processor design. By combining JOPcore, the Cyclone Board and BaseIO, a ready-to-use Java Processor system with Internet connection and industrial grade IO is available.

Other applications include Ethernet and industrial IO, like remote control and measurement.

All input and output pins are EMC/ESD protected and routed to robust connectors. Analog comparators can be used to build sigma delta A/D converters.

A step-down switching regulator with a large AC/DC input range is added for a flexible power supply.

Features

- Cirrus Logic CS8900 10Base-T Ethernet Controller
- Step-down SMPS for 8V to 24V AC/DC supply
- Possibility to power by battery and supervise this voltage
- RS232 9-pin male connector
- Ethernet RJ45 connector
- All IOs are available on 2 inch (5,08 mm) Phoenix connectors
- 10 EMC/ESD protected digital inputs
- 2 EMC/ESD protected analog inputs (4 to 20mA)
- 4 EMC/ESD protected digital outputs (open collector outputs)
- Expansion connector
- Small PCB size of 0.39 x 0.32 inch (99mm x 82mm)

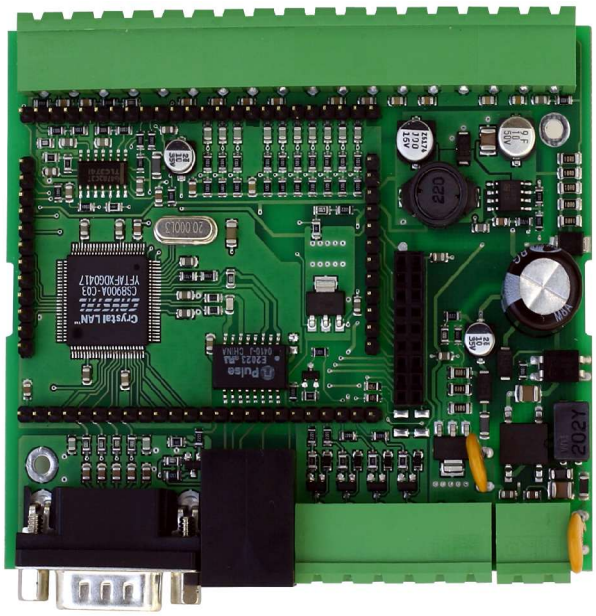

Figure 1: BaseIO without Cyclone Board

Details

PCB size:
99mm x 82mm (0.39 x 0.32 inch)

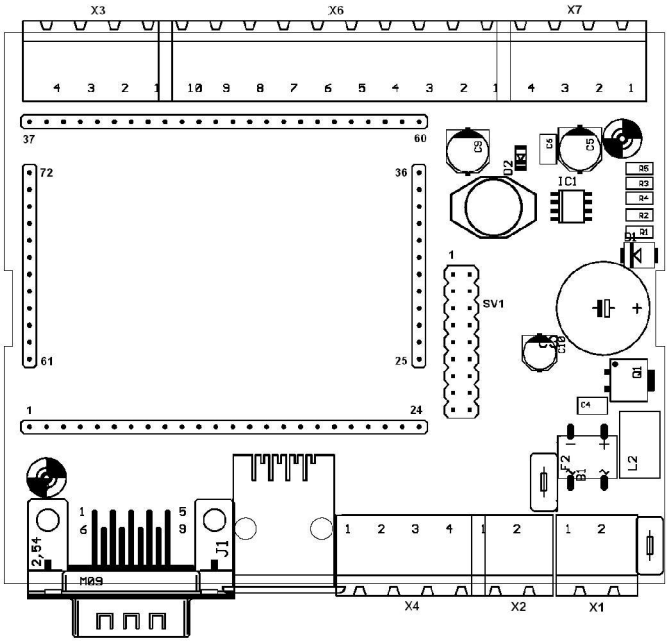

Figure 2: Simplified Place Plan

Power Supply

This board expects an AC or DC input voltage in the range from 8V to 24V. The rectified voltage is also available on connector X7 and can be supervised by the FPGA. In addition regulated 5V, with a maximal output current of approx. 100mA is provided on connector X3.

A regulated 3.3V voltage for the Cyclone Board is generated and is also available on the expansion connector SV1.

For applications with high availability even during main power loss, a 12 Volt lead acid battery can be connected to X2. An internal circuit charges the battery, if the board is connected to main power. The battery will automatically take over the supply when the main power fails and if the BAT signal (IO_L16) is high. To prevent a total discharge, the battery voltage can be supervised and switched off by setting the BAT signal to low.

Both power lines, from main and battery, are protected with a resettable fuse.

RS-232

The serial line from the MAX3232 on the Cyclone Board is connected to a 9-pin connector. It is protected against high-frequency interferences by passive filters. The DTR handshake signal is present on IO_L11 of the FPGA.

Ethernet

Ethernet Connector

This board is especially developed to provide a 10-Base-T Ethernet port for the Cyclone Board. A RJ45 connector and transformer are added in compliance to the IEEE802.3 standard.

Interface Controller

The LAN Controller CS8900A includes all basic function for communication with other Ethernet devices over the IEEE802.3 10-Base-T standard.

The following programmable tasks are implemented in the internal MAC engine.

- Collision detection and automatic retransmission
- Preamble generation and detection
- CRC generation and test
- Address filtering of received frames

Signal	Pin (FPGA)	Dir. (FPGA)
ISA_D0	IO_L2	IN/OUT
ISA_D1	IO_L3	IN/OUT
ISA_D2	IO_L4	IN/OUT
ISA_D3	IO_L5	IN/OUT
ISA_D4	IO_L6	IN/OUT
ISA_D5	IO_L7	IN/OUT
ISA_D6	IO_L8	IN/OUT
ISA_D7	IO_L9	IN/OUT
ISA_A0	IO_T6	OUT
ISA_A1	IO_T5	OUT
ISA_A2	IO_T4	OUT
ISA_A3	IO_T3	OUT
ISA_A4	IO_T2	OUT
ISA_RESET	IO_L10	OUT
ISA_NIOW	IO_L1	OUT
ISA_NIOR	IO_T1	OUT

Table 1: Ethernet ISA-Bus Signals

All configuration data as well as the transmitting and receiving data frames are stored in the internal memory. This is used by the application over the ISA-lines shown in Table 1. The ISA-Bus interface on this board is running in the I/O Mode described in the CS8900A data sheet. The base address of 0x0300h is permanently attached to the address bus. Because the interrupt signals are not used, the application has to poll the interrupt status queue for detecting a received frame.

Java sources for CS8900 driver and a simple TCP/IP stack are available and described in application notes.

Digital IO's

Input

There are 10 digital inputs on connector X6/7 available. Each of it features the circuit shown in Figure 3. It is intended for connecting floating switches.

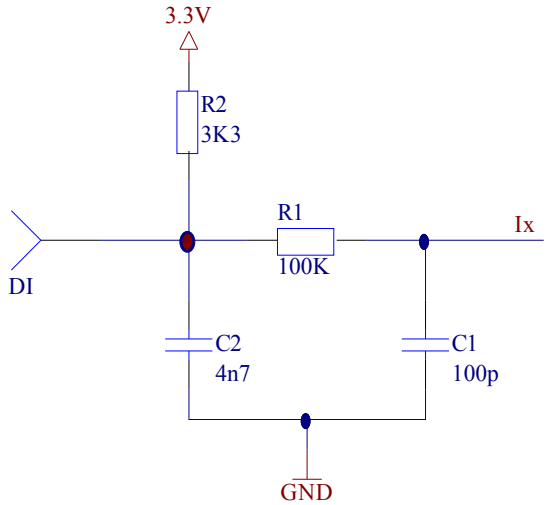

Figure 3: Digital Input Circuit

DI	Signal	Signal (FPGA)
1	I1	IO_R11
2	I2	IO_R12
3	I3	IO_R13
4	I4	IO_R14
5	I5	IO_R15
6	I6	IO_R16
7	I7	IO_R17
8	I8	IO_R18
9	I9	IO_R19
10	I10	IO_R20

Table 2: DI Signals

Output

The four digital outputs on connector X4 are open-collector with a recovery diode as shown in Figure 4. The maximum input current of the transistor is 100mA.

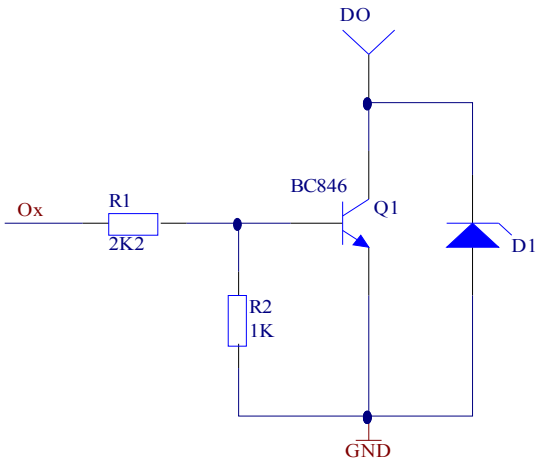

Figure 4: Digital Output Circuit

DO	Signal	Signal (FPGA)
1	O1	IO_L17
2	O2	IO_L18
3	O3	IO_L19
4	O4	IO_L20

Table 3: DO Signals

Analog Inputs

Two inputs on X3 are extended with simple A/D converters. A Sigma/Delta HDL core has to be implement in the FPGA in order to use the analog inputs.

Figure 5 shows the circuit and the corresponding block diagram. The reference voltage is half of VCC (3.3V). SDO is used to output a pulse-width-modulated signal. The ratio of low to high period (inverted because *adding* to the analog voltage) is proportional to the input voltage. To change the pulse-width the signal SDI is used. If it is low the pulse should be incremental reduced otherwise it should be increased.

Because the output voltage of the FPGA is maximum 3.3V, the converter voltage range amounts from around 0V to 3.3V. The 100 Ohms resistor is added to support a 4 to 20mA input current range. The sampling rate should be high enough that the capacitor works as integrator and low enough that the lifted voltage isn't too small. A practical value is around 600kHz. The result (one bit) has been taken for several samples to generate the desired resolution. The cut-off frequency depends on this resolution and is about 100Hz.

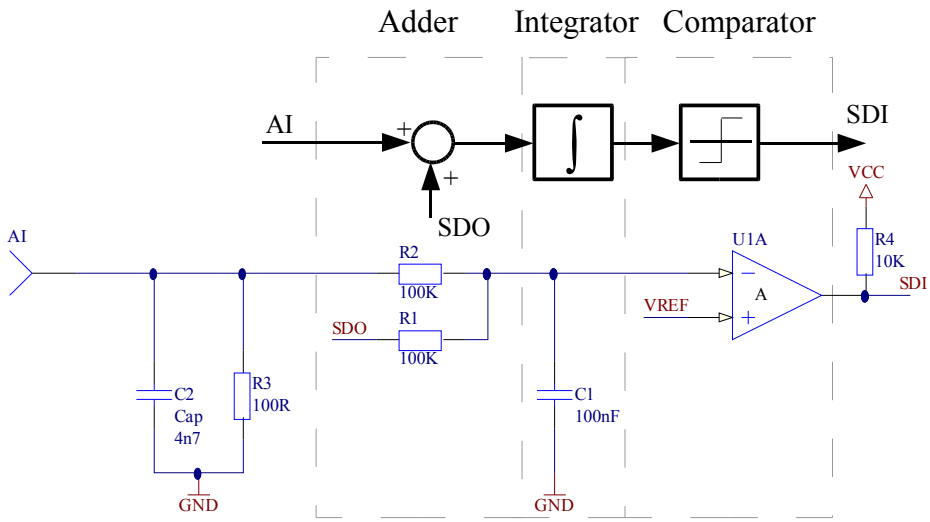

Figure 5: Sigma-Delta A/D

An example is given in the VHDL file called *sigdel.vhd* in the project tree.

There is a second A/D converter for supervising the power supply voltage. It is similar to the above described, but there is a voltage divider with a ratio of 1/11 in the analog line.

A/D	Signal	Signal (FPGA)	Dir. (FPGA)
1	SDI1	IO_R7	IN
	SDO1	IO_R4	OUT
2	SDI2	IO_R6	IN
	SDO2	IO_R5	OUT
Power	SDI3	IO_R8	IN
	SDO3	IO_R3	OUT

Table 4: A/D Signals

Expansion Connector

Another 18-pin connector SV1 with the pin assignment shown in Table 5 is provided as an expansion connector. The signals LAN and LINK are the lines from the LAN controller for status LED's. These are active-low, open-drain ports.

Pin	Signal	Signal (FPGA)
1	3.3V	-
2	GND	-
3	LO1	IO_B10
4	LO2	IO_B9
5	LO3	IO_B8
6	LO4	IO_B7
7	LO5	IO_B6
8	LO6	IO_B5
9	LO7	IO_B4
10	LO8	IO_B3
11	LO9	IO_B2
12	LO10	IO_B1
13	LO11	IO_L15
14	LO12	IO_L14
15	LO13	IO_L13
16	LO14	IO_L12
17	LAN	-
18	LINK	-

Table 5: Expansion connector

Summary of pin assignment

All signals should be set to LVCMOS level standard.

Connector	Pin	Signal
X1	1	~ VS
	2	~ VS
X2	1	+12V Batt.
	2	GND Batt.
X3	1	+5V Output
	2	Analog IN1
	3	Analog IN2
	4	GND
X4	1	Digital OUT1
	2	Digital OUT2
	3	Digital OUT3
	4	Digital OUT4
X6	1	Digital IN8
	2	Digital IN7
	3	Digital IN6
	4	Digital IN5
	5	GND
	6	Digital IN4
	7	Digital IN3
	8	Digital IN2
	9	Digital IN1
	10	GND
X7	1	+VS/Batt Output
	2	Digital IN10
	3	Digital IN9
	4	GND

Table 6: Pin assignment

Ordering Information

Package Contents

- TE0180-00 BaseIO
- Documentation CD-ROM

Ordering Number

The order number is: TE0181-00

History

Rev.	Date	Who	Description
0.9	2004-12-20	TS	Created
1.0	2005-01-22	FST	Revised

Table 7: History