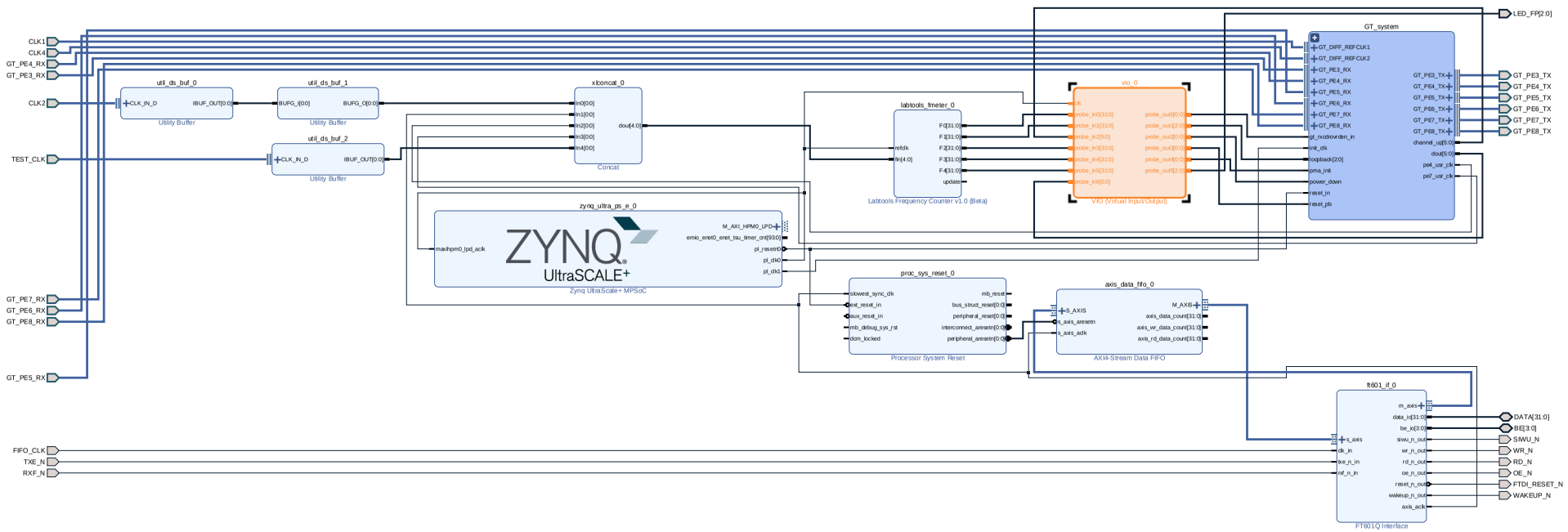
CLK1
CLK4
GT_PE4_RX
GT_PE3_RX
CLK2
TEST_CLK
GT_PE7_RX
GT_PE6_RX
GT_PE8_RX
GT_PE5_RX
FIFO_CLK
TXE_N
RXF_N
util_ds_buf_0
CLK_IN_D
IBUF_OUT[0:0]
Utility Buffer
util_ds_buf_1
BUFG_I[0:0]
BUFG_O[0:0]
Utility Buffer
util_ds_buf_2
CLK_IN_D
IBUF_OUT[0:0]
Utility Buffer
xlconcat_0
in0[0:0]
in1[0:0]
in2[0:0]
in3[0:0]
in4[0:0]
dout[4:0]
Concat
zynq_ultra_ps_e_0
ZYNQ
UltraSCALE+
Zynq UltraScale+ MPSoC
maxihpm0_lpd_aclk
M_AXI_HPM0_LPD
emio_enet0_enet_tsu_timer_cnt[93:0]
pl_resetn0
pl_clk0
pl_clk1
labtools_fmeter_0
refclk
fin[4:0]
F0[31:0]
F1[31:0]
F2[31:0]
F3[31:0]
F4[31:0]
update
Labtools Frequency Counter v1.0 (Beta)
vio_0
clk
probe_in0[31:0]
probe_in1[31:0]
probe_in2[5:0]
probe_in3[31:0]
probe_in4[31:0]
probe_in5[31:0]
probe_in6[5:0]
probe_out0[0:0]
probe_out1[2:0]
probe_out2[0:0]
probe_out3[0:0]
probe_out4[0:0]
probe_out5[2:0]
VIO (Virtual Input/Output)
GT_system
GT_DIFF_REFCLK1
GT_DIFF_REFCLK2
GT_PE3_RX
GT_PE4_RX
GT_PE5_RX
GT_PE6_RX
GT_PE7_RX
GT_PE8_RX
gt_rxcdrovrden_in
init_clk
loopback[2:0]
pma_init
power_down
reset_in
reset_pb
GT_PE3_TX
GT_PE4_TX
GT_PE5_TX
GT_PE6_TX
GT_PE7_TX
GT_PE8_TX
channel_up[5:0]
dout[5:0]
pe4_usr_clk
pe7_usr_clk
LED_FP[2:0]
proc_sys_reset_0
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
axis_data_fifo_0
S_AXIS
s_axis_aresetn
s_axis_aclk
M_AXIS
axis_data_count[31:0]
axis_wr_data_count[31:0]
axis_rd_data_count[31:0]
AXI4-Stream Data FIFO
ft601_if_0
m_axis
data_i[31:0]
be_o[3:0]
swu_n_out
wr_n_out
rd_n_out
oe_n_out
reset_n_out
wakeup_n_out
axis_aclk
s_axis
clk_in
txe_n_in
rxf_n_in
FT601Q Interface
DATA[31:0]
BE[3:0]
SWU_N
WR_N
RD_N
OE_N
FTDI_RESET_N
WAKEUP_N