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2 Overview

The Trenz Electronic TE0725 is a low cost small-sized FPGA module integrating a Xilinx Artix-7 (15-100T) and 32 MByte Flash memory for configuration and operation.

Refer to http://trenz.org/te0725-info for online version of this manual and the rest of available documentation of the product.

2.1 Key Features

- Xilinx Artix-7 XC7A35T (A15 to A100T)
- Commercial Temperature Grade (Industrial on Request)
- 32 MByte Flash Memory
- 2 x 50 Pin Headers with 2.54mm Pitch, Ideal for Breadboard Use
- 87 IOs (42 + 42 + 3)
- 100 MHz System Clock
- I2C EEPROM
- 3.3V Single Power Supply with On-Board Voltage Regulators
- Size 73 x 35 mm
- JTAG/UART Connector
- 2 LED’s
- Optional HyperRAM (8 to 32 MByte)
- Optional POF Fiber Optical Adapter (125/250 Mbps)

2.2 Block Diagram

2.3 Main Components

Note on the images below, that there is no POF transceiver, no 50-pin headers and no JTAG/UART header installed.
1. Xilinx Artix-7 FPGA, U1
2. 32-MByte Flash memory, U7
3. Enpirion EN6347 4A PowerSoC DC-DC step down converter, U10
4. Enpirion EN5311 1A PowerSoC synchronous buck regulator with integrated inductor, U11
5. POF transceiver placeholder, U8
6. 50-pin placeholder for breadboard connector, J1
7. 50-pin placeholder for breadboard connector, J2
8. JTAG/UART connector, JB1
9. Green LED D2(SYSLED) and red LED D3(DONE)
10. 16K x 8 (128-Kbit) serial EEPROM, U2
11. Low-noise, high PSRR, RF, 200-mA low-dropout linear regulator, U9
12. Ultra-low supply-current voltage monitor with optional watchdog, U6
13. Cypress S27KS0641 64-Mbit (8-MByte) HyperRAM™ self-refresh DRAM, U4
3 Signals, Interfaces and Pins

3.1 I/O Banks

<table>
<thead>
<tr>
<th>Bank</th>
<th>VCCIO</th>
<th>B2B I/O</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>3.3V</td>
<td>0</td>
<td>JTAG</td>
</tr>
<tr>
<td>14</td>
<td>3.3V</td>
<td>0 (3)</td>
<td>3 I/O in XMOD-JTAG - for use as UART</td>
</tr>
<tr>
<td>15</td>
<td>1.8V</td>
<td>0</td>
<td>used for optional hyper RAM</td>
</tr>
<tr>
<td>16</td>
<td>2.5V</td>
<td>0</td>
<td>used for optional optical fiber transceiver</td>
</tr>
<tr>
<td>34</td>
<td>User select</td>
<td>42</td>
<td>0R resistor option to select 3.3V</td>
</tr>
<tr>
<td>35</td>
<td>User select</td>
<td>42</td>
<td>0R resistor option to select 3.3V</td>
</tr>
</tbody>
</table>

3.2 JTAG Interface

JTAG access to the Xilinx Artix-7 device is provided through connector JB1.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Pin Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCK</td>
<td>JB1-4</td>
</tr>
<tr>
<td>TDO</td>
<td>JB1-8</td>
</tr>
<tr>
<td>TDI</td>
<td>JB1-10</td>
</tr>
<tr>
<td>TMS</td>
<td>JB1-12</td>
</tr>
</tbody>
</table>

Connector JB1 (2 x 6 pin header) is compatible with XMOD JTAG adapter TE0790. This adapter can be inserted from top onto the TE0725, if JB1 is fitted with male pin header. Optionally JB1 can be fitted with pin header from bottom, in that case the JTAG cable connector must be on the base board. When using XMOD-JTAG in JB1 then additionally USB UART is usable, and the push-button on XMOD works as configuration reset.

Recommended TE0790 (XMOD) DIP-switch settings :

- S2-1: ON
- S2-2: OFF
- S2-3: OFF
- S2-4: OFF

TE0790 can be in some cases used to power up TE0725 (other TE0790 DIP settings), however this is not recommended. TE0790-01 can not supply enough power for TE0725 (LED may blink but the module is not operating properly, especially in case of larger and more sophisticated designs).

3.3 POF Transceiver
### 3.4 On-board LED's

<table>
<thead>
<tr>
<th>LED Color</th>
<th>FPGA</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>D2</td>
<td>Green</td>
<td>M16</td>
</tr>
<tr>
<td>D3</td>
<td>Red</td>
<td>DONE Active low</td>
</tr>
</tbody>
</table>

### 3.5 Connectors

All connectors are for 100mil headers, all connector locations are in 100 mil grid.
4 Power and Power-On Sequence
To power-up a module, power supply with minimum current capability of 1A is recommended.

4.1 Power Supply
TE0725 needs one single power supply with nominal of 3.3V.

4.2 Power Consumption

<table>
<thead>
<tr>
<th>FPGA Design</th>
<th>Typical Power, 25C ambient</th>
</tr>
</thead>
<tbody>
<tr>
<td>A35T</td>
<td>Not configured TBD*</td>
</tr>
<tr>
<td>A35T</td>
<td>LED blinking</td>
</tr>
<tr>
<td>A100T</td>
<td>Not configured TBD*</td>
</tr>
</tbody>
</table>

*TBD - To Be Determined.

Actual power consumption depends on the FPGA design and ambient temperature.

4.3 Power-On Sequence
There is no specific or special power-on sequence, single power source is needed as VIN, rest of the sequence is automatic.
5 Variants Currently In Production

Trenz shop TE0725 overview page

English page  German page
6 Technical Specifications

6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Reference document</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V supply voltage</td>
<td>-0.1</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>HR I/O banks supply voltage (VCCO)</td>
<td>-0.5</td>
<td>3.6</td>
<td>V</td>
<td>Xilinx datasheet DS181</td>
</tr>
<tr>
<td>HR I/O banks input voltage</td>
<td>-0.4</td>
<td>VCCO + 0.55</td>
<td>V</td>
<td>Xilinx datasheet DS181</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-40</td>
<td>+85</td>
<td>°C</td>
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6.2 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Reference document</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN supply voltage</td>
<td>3.135</td>
<td>3.45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>HR I/O banks supply voltage (VCCO)</td>
<td>1.14</td>
<td>3.465</td>
<td>V</td>
<td>Xilinx datasheet DS181</td>
</tr>
<tr>
<td>HR I/O banks input voltage</td>
<td>-0.20</td>
<td>VCCO + 0.20</td>
<td>V</td>
<td>Xilinx datasheet DS181</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>0</td>
<td>+85</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

⚠️ Please check Xilinx datasheet DS181 for complete list of absolute maximum and recommended operating ratings for the Artix-7 device.

6.3 Physical Dimensions

Please note that two different units are used on the figures below, SI system millimeters (mm) and imperial system thousandths of an inch(mil). This is because of the 100mil pin headers used, see also explanation below. To convert mils to millimeters and vice versa use formula 100mil's = 2.54mm.
All 100 mil pin headers are in 100 mil grid, the M3 mounting holes are in 50 mil grid aligned to the centers of the 100mil headers. The module is symmetrical, turning it 180 degrees will keep all I/O and Power pins in both 50 pin headers in compatible places.

6.4 Operating Temperature Ranges

Commercial grade modules
All parts conform to at least commercial temperature range of 0°C to +70°C.

**Industrial grade modules**

All parts are at least industrial temperature range of -40°C to +85°C.

The module operating temperature range depends on customer design and cooling solution. Please contact us for options.
7 Revision History

7.1 Hardware Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Notes</th>
<th>PCN</th>
<th>Documentation Link</th>
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<tr>
<td>2016-12-09</td>
<td>03</td>
<td>Second production release</td>
<td>TE0725-03</td>
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<tr>
<td>-</td>
<td>02</td>
<td>First production release</td>
<td>TE0725-02</td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>01</td>
<td>Prototypes</td>
<td></td>
<td></td>
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</table>

Hardware revision number is printed on the PCB board together with the module model number separated by the dash.

7.2 Document Change History

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Contributors</th>
<th>Description</th>
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<tbody>
<tr>
<td>2018-01-11</td>
<td>v.65</td>
<td>John Hartfiel</td>
<td>• Replace Links</td>
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<tr>
<td>2017-06-07</td>
<td>v.60</td>
<td>Jan Kumann</td>
<td>• Minor formatting</td>
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<tr>
<td>2017-01-27</td>
<td>v.57</td>
<td>Jan Kumann</td>
<td>• New block diagram</td>
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<tr>
<td>2017-01-12</td>
<td>v.46</td>
<td>Jan Kumann</td>
<td>• Revision 03 product images added</td>
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<tr>
<td>2016-12-15</td>
<td></td>
<td>Thorsten Trenz</td>
<td>• Hardware revision 03 specific information added</td>
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<tr>
<td>2016-12-09</td>
<td>v.40</td>
<td>Jan Kumann</td>
<td>• Hardware revision 02 block diagram added</td>
</tr>
<tr>
<td>2016-12-02</td>
<td>v.1</td>
<td>Antti Lukats</td>
<td>• Initial version</td>
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</tbody>
</table>
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Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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**WEEE**


Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

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