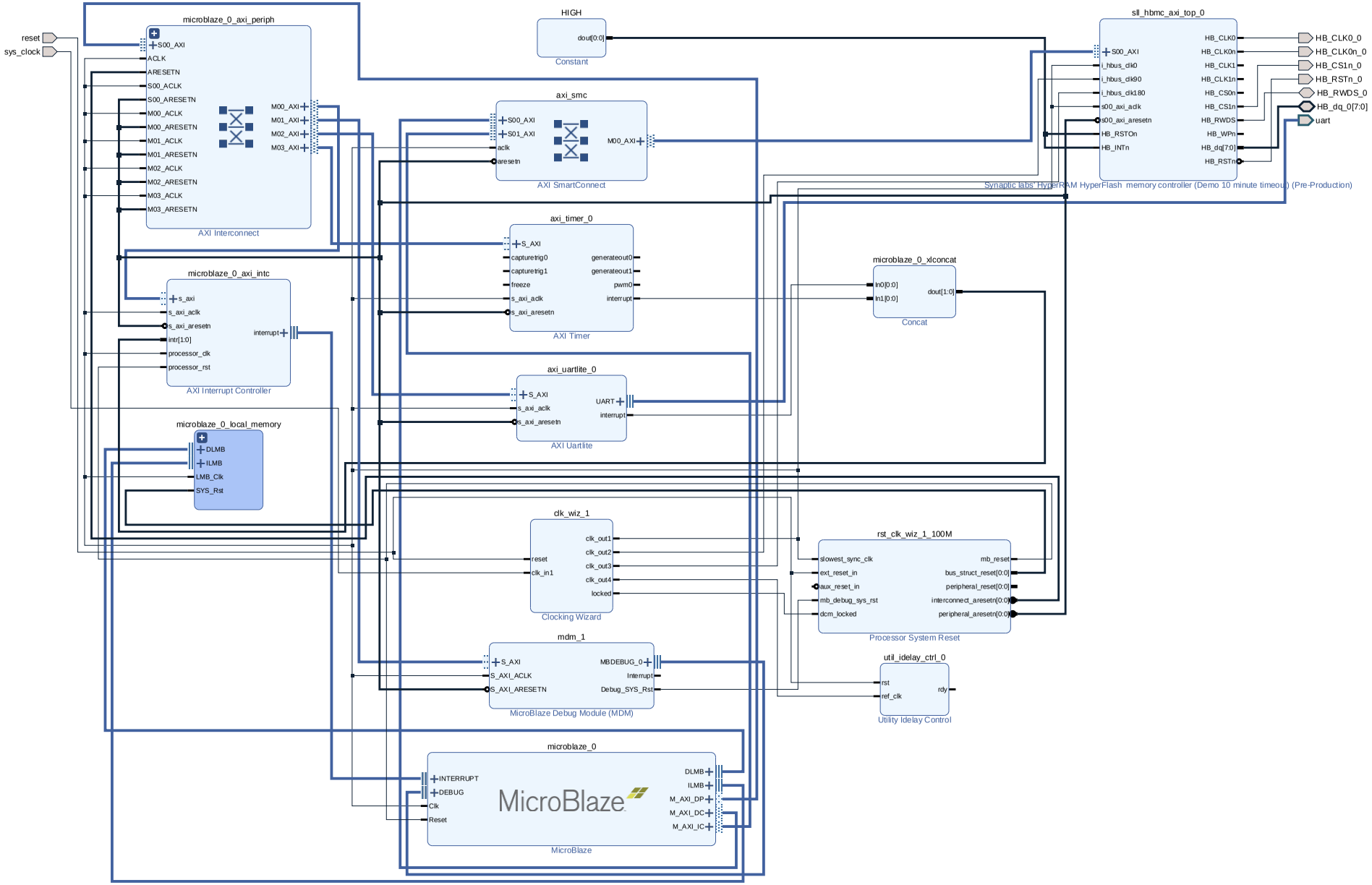
reset
sys_clock
microblaze_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M02_ACLK
M02_ARESETN
M03_ACLK
M03_ARESETN
M00_AXI
M01_AXI
M02_AXI
M03_AXI
AXI Interconnect
HIGH
dout[0:0]
Constant
axi_smc
S00_AXI
S01_AXI
aclk
aresetn
M00_AXI
AXI SmartConnect
sll_hbmc_axi_top_0
S00_AXI
i_hbus_clk0
i_hbus_clk90
i_hbus_clk180
s00_axi_aclk
s00_axi_aresetn
HB_RSTOn
HB_INTn
HB_CLK0
HB_CLK0n
HB_CLK1
HB_CLK1n
HB_CS0n
HB_CS1n
HB_RWDS
HB_WPn
HB_dq[7:0]
HB_RSTn
Synaptic labs' HyperRAM HyperFlash memory controller (Demo 10 minute timeout) (Pre-Production)
HB_CLK0_0
HB_CLK0n_0
HB_CS1n_0
HB_RSTn_0
HB_RWDS_0
HB_dq_0[7:0]
uart
axi_timer_0
S_AXI
capturetrig0
capturetrig1
freeze
s_axi_aclk
s_axi_aresetn
generateout0
generateout1
pwm0
interrupt
AXI Timer
microblaze_0_xlconcat
In0[0:0]
In1[0:0]
dout[1:0]
Concat
microblaze_0_axi_intc
s_axi
s_axi_aclk
s_axi_aresetn
intr[1:0]
processor_clk
processor_rst
interrupt
AXI Interrupt Controller
axi_uartlite_0
S_AXI
s_axi_aclk
s_axi_aresetn
UART
interrupt
AXI Uartlite
microblaze_0_local_memory
DLMB
ILMB
LMB_Clk
SYS_Rst
clk_wiz_1
reset
clk_in1
clk_out1
clk_out2
clk_out3
clk_out4
locked
Clocking Wizard
rst_clk_wiz_1_100M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
mdm_1
S_AXI
S_AXI_ACLK
S_AXI_ARESETN
MBDEBUG_0
Interrupt
Debug_SYS_Rst
MicroBlaze Debug Module (MDM)
util_idelay_ctrl_0
rst
ref_clk
rdy
Utility Idelay Control
microblaze_0
INTERRUPT
DEBUG
Clk
Reset
MicroBlaze
DLMB
ILMB
M_AXI_DP
M_AXI_DC
M_AXI_IC
MicroBlaze