Special notes:

J M2 pin 54: VCCIO_0 is input (3.3V/2.5V)
Changes REV 02:
1. Added 0 ohm strap option to supply VCCIO0 on B2B connector
2. Added PCB Revision sense support. PCB Revision readout possible from HDL Design
3. Updated FPGA pin PROG_B connection. TPS3805H33 push-pull output RESET_N not affected on baseboard circuit, connected to PROG_B.
4. C8, C54, C56 updated to 100uF for variant 50-2I
5. Added testpoints

Changes REV 02A (12.2018):
1. New FLASH memory U7 S25FL127SABMFV10

Changes REV 03:
1) Changed obsolete component U3 (LXDC2HL18A-052 -> EP5357HUI)
2) DXP/DXN connected to GND (recommendation UG475, p31)
3) Added serial number to silks
4) Changed obsolete component Q1 (TPS27082LDIDCR -> TPS27081ADDICR)
5) Full update LIB
6) Optimized testpoints placement