Product Change Notification
Trenz Electronic TE0600 modules

Notification Title
Trenz Electronic TE0600 module, new board revision.

Notification Type
Hardware Revision

Notification Entity

<table>
<thead>
<tr>
<th>minor change</th>
<th>major change</th>
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<tbody>
<tr>
<td></td>
<td>●</td>
</tr>
</tbody>
</table>

Products Affected
Trenz Electronic TE0600 series.
New 02 revision will completely replace 01 revision. To buy 01 revision modules, contact Trenz Electronic representative.

Description of Change
New board revision with new capabilities and features:
● More powerful regulators for 1.2V and 1.5V rails
● VCCAUX separated from 2.5V power rail
● 128Mbit SPI Flash
● Additional secure 1Kbit EEPROM
● Optional B2B connection to bank 2 differential clock input
● New memory options

Reason for Change
Increasing product power characteristics. New connectivity and security features for user projects.

Impact
As new SPI Flash used in new board revision, flash related operation should be changed.
**ISE iMPACT Software**

For indirect SPI flash programming W25Q128BV SPI PROM should be selected.

![Select Attached SPI/BPI](image)

**User firmware**

**New SPI Flash have differ Device ID**

<table>
<thead>
<tr>
<th>Module revision</th>
<th>Manufacturer ID</th>
<th>Device ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revision 01</td>
<td>0xEF (Winbond)</td>
<td>0x16 (W25Q64CV)</td>
</tr>
<tr>
<td>Revision 02</td>
<td>0xEF (Winbond)</td>
<td>0x17 (W25Q128BV)</td>
</tr>
</tbody>
</table>

**Table 1: SPI Device ID**

**Additional chip on 1-Wire bus**

To work with multiple chips on 1-Wire bus firmware should perform search algorithm [http://www.maximintegrated.com/app-notes/index.mvp/id/187](http://www.maximintegrated.com/app-notes/index.mvp/id/187) to find address of each chip and use MACH_ROM commands to work with selected chip.

**Revision encoding**

Module revision coded by 4 FPGA BR[3:0] pins, which can be read by FPGA firmware. All these pins should be configure to have internal PULLUP.

<table>
<thead>
<tr>
<th>Signal FPGA pin</th>
<th>BR3</th>
<th>BR2</th>
<th>BR1</th>
<th>BR0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revision 01</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Revision 02</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Table 2: Board revisions pin coding**

**New revision advantages**

- Projects with higher power consumption possible
- More convenient eFUSE usage
- More Flash memory for user data
- Security option for devices without eFUSE
- Differential clock input option for FPGA bank 2

For complete module information refer TE0600 user manual.

Expected Sample Availability Date
First Availability of Post-Conversion Product November 2012.

Expected Production Availability Date
First Availability of Post-Conversion Product January 2013.

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