Overview

Trenz Electronic GigaBee XC6SLX series are industrial-grade FPGA micromodules integrating a leading-edge Xilinx Spartan-6 LX FPGA, Gigabit Ethernet transceiver (physical layer), two independent banks of 16-bit-wide 128/512 MBytes DDR3 SDRAM, 16 MBytes SPI Flash memory for configuration and operation, and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via robust board-to-board (B2B) connectors. All this on a tiny footprint, smaller than half a credit card, at the most competitive price. Hardware and software development environment, as well as reference designs are available at: www.trenz-electronic.de.

Sample Applications

- Cryptographic hardware module
- Digital signal processing
- Embedded educational platform
- Embedded industrial OEM platform
- Embedded system design
- Emulation platforms
- FPGA graphics
- Image processing
- IP (intellectual property) cores
- Low-power design
- Parallel processing
- Rapid prototyping
- Reconfigurable computing
- System-on-Chip (SoC) development
Key Features

- Industrial-grade Xilinx Spartan-6 LX FPGA micromodule (LX45 / LX100 / LX150)
- 10/100/1000 tri-speed Gigabit Ethernet transceiver (PHY)
- 2 x 16-bit-wide 1 Gb (128 MB) or 4Gb (512 MB) DDR3 SDRAM
- 128Mb (16 MB) SPI Flash memory (for configuration and operation) accessible through:
  - 1Kb Protected 1-Wire EEPROM with SHA-1 Engine
  - JTAG port (SPI indirect)
- FPGA configuration through:
  - B2B connector
  - JTAG port
  - SPI Flash memory
- Plug-on module with 2 x 100-pin high-speed hermaphroditic strips
- Up to 52 differential, up to 109 single-ended (+ 1 dual-purpose) FPGA I/O pins available on B2B strips
- 4.0 A x 1.2 V power rail
- 1.5 A x 1.5 V power rail
- 125 MHz reference clock signal
- Single-ended custom oscillator (option)
- eFUSE bit-stream encryption (LX100 or larger)
- 1 user LED
- Evenly-spread supply pins for good signal integrity
- Other assembly options for cost or performance optimization available upon request.
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1 Technical Specifications

1.1 Components

- Xilinx Spartan-6 LX FPGA:
  - XC6SLX45-2FGG484C = 43 K logic cells, commercial grade
  - XC6SLX45-2FGG484I = 43 K logic cells, industrial grade
  - XC6SLX100-2FGG484C = 101 K logic cells, commercial grade
  - XC6SLX100-2FGG484I = 101 K logic cells, industrial grade
  - XC6SLX150-2FGG484C = 147 K logic cells, commercial grade
  - XC6SLX150-2FGG484I = 147 K logic cells, industrial grade
- 10/100/1000 Gigabit Ethernet transceiver (physical layer)
  - Marvell Semiconductor 88E1111
- 2 × independent 16-bit-wide (data-bus) 1 Gigabit (128 megabyte) or 4 Gigabit (512 megabyte) DDR3 SDRAM
- 128 megabit (16 megabyte) serial Flash memory with dual/quad SPI interface
- 48-bit node address chip
  - Maxim Integrated Products DS2502-E48
- 1Kb Protected 1-Wire EEPROM with SHA-1 Engine
  - Maxim Embedded Security Products DS2432
- 2 x fine-pitch (0.5 mm) 100-pin high-speed (up to 10.0 GHz / 20 Gbps) hermaphroditic strips
- Up to 52 differential FPGA input/output pins available on B2B strips
- Up to 109 single-ended (+ 1 dual-purpose) FPGA input/output pins available on B2B strips
- Ethernet (PHY), JTAG and SPI pins available on B2B strips
- 4.0 A high-efficiency DC-DC switching regulator for power rail 1.2V
- 1.5 A high-efficiency DC-DC switching regulator for power rail 1.5V
- 2 x 800 mA DC-DC linear regulator for power rails 2.5V and VCCAUX
- Processor supervisory circuits with power-fail and watchdog
  - Texas Instruments TPS3705-33
- 125 MHz clock signal (system + user)
- Footprint for custom single-ended oscillator (option)
- 1 x LED (user)
- Power supply voltage: 3.3 V
- Power supply source: board-to-board interconnect (e.g. carrier board)
- Dimensions: 50 mm × 40 mm (20 cm²)
- Minimum module height: 8 mm (without connectors)
- Maximum height on carrier board surface: ≈ 13 mm (standard connectors)
- Minimum height on carrier board surface: ≈ 5 mm (standard connectors)
- Weight: 17.2 ± 0.1 g
- Temperature grades:
  - commercial (C-type FPGA device)
  - industrial (I-type FPGA device)

### 1.2 Dimensions

![GigaBee board dimensions (top view)](image)

GigaBee XC6SLX can reach a minimum vertical height of about 8 mm, if B2B
connectors are not assembled. The maximum component height on the module board on the top side is about 3.5 mm. The maximum component height on the module board on the bottom side is about 3.0 mm.

The typical minimum and maximum height from the carrier board surface, of a GigaBee XC6SLX when it mounted on a carrier board, is respectively about 5.0 mm and about 13 mm.

GigaBee XC6SLX has 4 mounting holes, one in each corner. The module can be fixed by screwing M3 screws (ISO 262) onto a carrier board through those mounting holes.

GigaBee XC6SLX weighs between 17.1 and 17.3 g with standard connectors.

### 1.3 Power Consumption

Power consumption of GigaBee XC6SLX modules highly depend on the FPGA design implemented. Some typical power consumptions are provided in Table 1 for the following reference systems:

- Boards – GigaBee XC6SLX 45/100/150
- Base board – TE0603-02
- Power supply – 5 V from baseboard
- Connected Gigabit Ethernet cable

<table>
<thead>
<tr>
<th>FPGA type</th>
<th>Unconfigured</th>
<th>Configured with Web-server reference design</th>
</tr>
</thead>
<tbody>
<tr>
<td>LX45</td>
<td>0.15 A</td>
<td>0.6 A</td>
</tr>
<tr>
<td>LX100</td>
<td>0.17 A</td>
<td>0.5 A</td>
</tr>
<tr>
<td>LX150</td>
<td>0.2 A</td>
<td>0.5 A</td>
</tr>
</tbody>
</table>

**Table 1: Power consumption**
2 Detailed Description

2.1 Block Diagram

Figure 4 shows a block diagram of the GigaBee XC6SLX board.

![Block Diagram](image)

Figure 4: TE0600-02 Block Diagram

2.2 Power Supply

The nominal supply voltage of the GigaBee XC6SLX is 3.3 volt. The minimum supply voltage is 3.0 volt. The maximum supply voltage is 3.45 volt.

Supply voltages beyond the range might affect to device reliability, or even cause permanent damage of the device!

Board power supply diagram is shown in Figure 5.
2.2.1 Power Supply Sources

GigaBee XC6SLX board must be powered at least in one of the following two ways:

- through B2B connector J1 (pins 1, 3, 5, 7, 9, 11, 13, 15),
- through B2B connector J2 (pins 2, 4, 6, 8, 10, 12).

We recommend to supply the module with all these 14 pins. When one or more of these pins are not power supplied, it or they can be used as power source for user applications.

Please make sure that your logic design does not draw more RMS current per pin than specified in section 2.4 Board-to-board Connectors.

2.2.2 FPGA banks VCCIO power supply

FPGA VCCIO power options shown in Table 2. Default values for configurable voltages shown in braces.

<table>
<thead>
<tr>
<th>Bank</th>
<th>Supply voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>B0</td>
<td>VCCIO 0 (3.3 V)</td>
</tr>
<tr>
<td>B1</td>
<td>VCCIO 1 (1.5 V)</td>
</tr>
<tr>
<td>B2</td>
<td>3.3 V</td>
</tr>
<tr>
<td>B3</td>
<td>1.5 V</td>
</tr>
</tbody>
</table>

Table 2: FPGA banks VCCIO power supply

Bank 0 power supply VCCIO 0 can be configured by user to 3.3 V, 2.5 V or
1.5 V, see Chapter 2.2.3.6 VCCIO0 Power Rail. Bank 1 VCCIO supply voltage is configured to 1.5 V to communicate with DDR3 SDRAM memory chip.¹

2.2.3 On-board Power Rails

GigaBee XC6SLX has the following power rails on-board.

2.2.3.1 3.3V Power Rail

It is the main internal power rail and must be supplied from an external power source.

It supplies the other following power rails:
- 1.2V / 4 A on-board high-efficiency switching voltage regulator;
- 1.5V / 1.5 A on-board high-efficiency switching voltage regulator;
- 2.5V 0.8 A linear voltage regulator;
- VCCIO0 power rail (option) (if zero-resistor R80 is not populated and zero-resistor R79 is populated).

2.2.3.2 1.2V Power Rail

It is converted from the 3.3V rail by a switching voltage regulator and can provide up to 4.0 A to:
- FPGA VCCINT power supply pins;
- Ethernet PHY;
- J1 connector.

2.2.3.3 1.5V Power Rail

It is converted from the 3.3V rail by a switching voltage regulator and can provide up to 1.5 A to:
- DDR3 SDRAM;
- Vref1 / Vref2 DDR3 SDRAM reference voltages;
- FPGA bank 3 VCCO;
- J1 connector.

2.2.3.4 2.5V Power Rail

It is converted from the 3.3V rail by a linear voltage regulator and can provide up to 0.8 A to:
- VCCAUX power rail;
- Ethernet physical layer;
- J1 connector;

¹ By special request modules can be supplied without DDR3 SDRAM chips. Contact Trenz Electronic support for details.
2.2.3.5 VCCAUX Power Rail

It is converted from the 3.3V rail by a linear voltage regulator and can provide up to 0.8 A to:

- FPGA auxiliary circuits;
- J2 connector.

2.2.3.6 VCCIO0 Power Rail

There are 4 options to supply this rail:

- from 3.3 V power rail (if zero-resistor R79 is populated and R80 is not);
- from 2.5 V power rail (if zero-resistor R80 is populated and R79 is not);
- from 1.5 V power rail (if zero-resistors R79 and R80 are not populated and VCCIO0 connected to 1.5 V power rail);
- from an external power source through J2 B2B connector (pins 1, 3, 5, 7, 9) (if R79 and R80 are not populated)

It supplies:

- FPGA bank 0 $V_{CCO}$.

Figure 6 show simplified schematic of power options. Dashed resistors are not populated by default.

---

2 Default assembling for VCCIO0 rail
Table 3 summarizes power rails information.

<table>
<thead>
<tr>
<th>power-rail name</th>
<th>nominal voltage(V)</th>
<th>maximum current (A)</th>
<th>power source</th>
<th>system supply</th>
<th>user supply</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V</td>
<td>3.3</td>
<td>2.4 (3.3 option)</td>
<td>J1, J2</td>
<td>module</td>
<td>J1 (≤1.2 A) J2 (≤1.2 A, ≤2.1 option)</td>
</tr>
<tr>
<td>2.5V</td>
<td>2.5</td>
<td>0.8</td>
<td>3.3V • linear</td>
<td>Ethernet</td>
<td>J1 (≤0.3 A) J2 (option)</td>
</tr>
<tr>
<td>1.5V</td>
<td>1.5</td>
<td>1.5</td>
<td>3.3V • switch.</td>
<td>DDR3 SDRAM VCCO (1+3)</td>
<td>J1 (≤0.3 A)</td>
</tr>
<tr>
<td>1.2V</td>
<td>1.2</td>
<td>4.0</td>
<td>3.3V • switch.</td>
<td>VCCINT Ethernet</td>
<td>J1 (≤0.6 A)</td>
</tr>
<tr>
<td>VCCAUX</td>
<td>2.5</td>
<td>0.8</td>
<td>3.3V • linear</td>
<td>FPGA</td>
<td>J2 (≤0.3 A)</td>
</tr>
<tr>
<td>VCCCI00</td>
<td>1.2, 1.5, 1.8, 2.5, 3.3</td>
<td>0.9</td>
<td>J2</td>
<td>VCCO (0)</td>
<td>J2 (≤0.9 A)</td>
</tr>
</tbody>
</table>

Table 3: On-board power rails summary

2.3 Power Supervision

2.3.1 Power-on Reset

During power-on, the /RESET line is first asserted. Thereafter, the supply voltage supervisor monitors the power supply rail 3.3V and keeps the /RESET line active (low) as long as the supply rail remains below the threshold voltage (2.93 volt). An internal timer delays the return of the /RESET line to the inactive state (high) to ensure proper system reset prior to a regular system start-up. The typical delay time $t_d$ of 200 ms starts after the supply rail has risen above the threshold voltage.

Figure 7: Reset on power-on
After this delay, the /RESET line is reset (high) and the FPGA configuration can start. When the supply rail voltage drops below the threshold voltage, the /RESET line becomes active (low) again and stays active (low) as long as the rail voltage remains below the threshold voltage (2.93 volt). Once the rail voltage raises again and remains over the threshold voltage for more than the typical delay time \( t_d \) of 200 ms, the /RESET line returns to the inactive state (high) to allow a new system start-up.

![Figure 8: Reset on power drop](image)

### 2.3.2 Power Fail

GigaBee XC6SLX integrates a power-fail comparator which can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply 3.3 V. When the voltage of the PFI (power-fail comparator input, input pin 16 of connector J2) line drops below 1.25 volt, the /PFO (power-fail comparator output, FPGA pin A2, label IO_L83P_3) line becomes active (low). The user application can sense this line to take action. To set a power fail threshold higher than 1.25 volt, the user can implement a simple resistive voltage divider on the carrier board.

### 2.4 Board-to-board Connectors

GigaBee XC6SLX mounts two Samtec Razor Beam LSHM connectors (J1 and J2) on the bottom side.

Each connector features the following characteristics:

- rows per connector: 2
- contacts per row: 50
- contacts per connector: 100
- connector gender: hermaphrodite
- pitch: 0.50 mm = 19.7 mil = .0197"
- mated height: min. 5.0 mm | typ. 8.0 mm | max. 12.0 mm
- mating force: min. 39 N | typ. 59 N | max. 62 N
- un-mating force: min. 49 N | typ. 73 N | max. 74 N
The overall number of connector contacts on the GigaBee XC6SLX is 200.

Samtec Razor Beam LSHM is a high-speed interconnect system with very fine pitch (50 mil) and low profile design. Razor Beam connectors are well suited for high speed applications with performance up to 11.5 GHz (23 Gb/s) at -3 dB insertion loss. Razor Beam contacts are ideal for high speed and rugged applications featuring undercut retention notches that increase the withdrawal force and provide an audible click when the contacts engage. In addition, the self-mating (hermaphroditic) design can help reduce inventory costs. The LSHM Series features also optional shielding for EMI protection (default on GigaBee XC6SLX).

Samtec Razor Beam LSHM connectors are keyed. On the bottom side of the GigaBee XSL6, the connectors are assembled in such a way to prevent the module to be reverse mounted on carrier boards.

Samtec Razor Beam LSHM are available in different lead styles, see Table 4 for details.

<table>
<thead>
<tr>
<th>lead style</th>
<th>A [mm]</th>
<th>B [mm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>−02.5</td>
<td>3.95</td>
<td>1.00</td>
</tr>
<tr>
<td>−03.0</td>
<td>4.45</td>
<td>1.50</td>
</tr>
<tr>
<td>−04.0</td>
<td>5.45</td>
<td>2.50</td>
</tr>
<tr>
<td>−06.0</td>
<td>7.45</td>
<td>4.50</td>
</tr>
</tbody>
</table>

Table 4: Samtec Razor Beam LSHM lead styles

Trenz Electronic recommends the same part as mating connector, due to its self-mating capability.

The Samtec Razor Beam LSHM series offers a variety of mated heights from 5.0 mm to 12.0 mm. Two mated standard GigaBee XC6SLX connectors have a typical mated height of 8.0 mm. Processing conditions will affect the following heights.

<table>
<thead>
<tr>
<th>standard connector lead style</th>
<th>mating connector lead style</th>
<th>mated height [mm]</th>
<th>min. height from carrier board [mm]</th>
<th>max. height on carrier board [mm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>–04.0</td>
<td>–02.5</td>
<td>6.5</td>
<td>≈ 3.5</td>
<td>≈ 11.5</td>
</tr>
<tr>
<td>–04.0</td>
<td>–03.0</td>
<td>7.0</td>
<td>≈ 4.0</td>
<td>≈ 12.0</td>
</tr>
<tr>
<td><strong>–04.0</strong></td>
<td><strong>–04.0</strong></td>
<td><strong>8.0</strong></td>
<td><strong>≈ 5.0</strong></td>
<td><strong>≈ 13.0</strong></td>
</tr>
<tr>
<td>–04.0</td>
<td>–06.0</td>
<td>10.0</td>
<td>≈ 7.0</td>
<td>≈ 15.0</td>
</tr>
</tbody>
</table>

Table 5: Samtec Razor Beam LSHM mated heights
Ordering codes for connectors J1 and J2 used in GigaBee XC6SLX board, and their mating connectors are given in Table 6.

<table>
<thead>
<tr>
<th>lead style</th>
<th>gender</th>
<th>Samtec</th>
<th>Trenz Electronic</th>
</tr>
</thead>
<tbody>
<tr>
<td>–02.5</td>
<td>hermaphroditic</td>
<td>LSHM-150-02.5-L-DV-A-S-K-TR</td>
<td>23836</td>
</tr>
<tr>
<td>–03.0</td>
<td>hermaphroditic</td>
<td>LSHM-150-03.0-L-DV-A-S-K-TR</td>
<td>23837</td>
</tr>
<tr>
<td>–04.0</td>
<td>hermaphroditic</td>
<td>LSHM-150-04.0-L-DV-A-S-K-TR</td>
<td>23838</td>
</tr>
<tr>
<td>–06.0</td>
<td>hermaphroditic</td>
<td>LSHM-150-06.0-L-DV-A-S-K-TR</td>
<td>23839</td>
</tr>
</tbody>
</table>

Table 6: Ordered codes of recommended B2B connectors

2.4.1 Connector Speed Rating

Samtec provides speed rating data for the Samtec Razor Beam LSHM connector system. The data presented in Table 7 are applicable only to the maximum and minimum mated heights. The speed rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signalling environment.

<table>
<thead>
<tr>
<th>mated height</th>
<th>5 mm</th>
<th>12 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>single-ended</td>
<td>11.5 GHz</td>
<td>7.5 GHz</td>
</tr>
<tr>
<td></td>
<td>23.0 Gb/s</td>
<td>15.0 Gb/s</td>
</tr>
<tr>
<td>differential</td>
<td>7.0 GHz</td>
<td>6.5 GHz</td>
</tr>
<tr>
<td></td>
<td>14.0 Gb/s</td>
<td>13.0 Gb/s</td>
</tr>
</tbody>
</table>

Table 7: Connectors speed rating

More details can be found in the Samtec Razor Beam LSHM series overview (“High Speed Characterization Reports”).

2.5 EPROM

GigaBee XC6SLX board contains a Maxim DS2502-E48 node address chip with factory-programmed valid MAC-48 address and 768 bits of OTP-EPROM memory for user data.

Address chip provide convenient data access through 1-Wire interface up to 16.3 kbps (FPGA pin T11).

More information can be found in the Maxim DS2502-E48 product overview.

Additional 1Kb protected 1-Wire EEPROM with SHA-1 engine DS2432 accessible via the same line.

More information can be found at the Maxim DS2432 product page.

2.6 DDR3 SDRAM Memory

The board contains two 1 Gb (128 MB) or 4 Gb (512 MB) DDR3 SDRAM chips. Data width of each chip is 16 bit. DDR3 memory connected to FPGA bank 1 and FPGA bank 3. Spartan-6 Memory controller Blocks operations can be merged to implement effective 32-bit memory interface. Refer Xilinx XAPP496 for detailed information.
2.7 Flash Memory

GigaBee XC6SLX board contains 128 Mb (16 MB) serial flash memory chip Winbond W25Q128BV (U11). This serial flash chip can operate as general SPI memory mode and in double or quad modes. Usage of dual and quad modes increase bandwidth up to 40 MB/s.

For more information see Winbond W25Q128BV product overview.

Flash can be programmed in several ways:

- Direct SPI programming via J1 connector.
- Indirect SPI programming via FPGA pins, controlled by JTAG.
- Direct SPI programming by FPGA, using SPI core.

Serial flash is connected to FPGA bank 2 and B2B connector J1; used pins are listed in Table 8.

<table>
<thead>
<tr>
<th>Flash signal</th>
<th>FPGA pin</th>
<th>J1 pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>/CS</td>
<td>T5</td>
<td>87</td>
</tr>
<tr>
<td>CLK</td>
<td>Y21</td>
<td>91</td>
</tr>
<tr>
<td>DI(IO0)</td>
<td>AB20</td>
<td>95</td>
</tr>
<tr>
<td>DO(IO1)</td>
<td>AA20</td>
<td>93</td>
</tr>
<tr>
<td>/WP(IO2)</td>
<td>U14</td>
<td>99</td>
</tr>
<tr>
<td>/HOLD(IO3)</td>
<td>U13</td>
<td>97</td>
</tr>
</tbody>
</table>

Table 8: Serial flash signals connection

2.8 Ethernet

The board contains a Marvell Alaska Ethernet PHY chip (88E1111) operating at 10/100/1000 Mb/s. The board supports GMII interface mode with the FPGA.

Configuration details:

- PHY address – 00111
- Advertise pause
- Auto Neg
- Advertise all caps
- Prefer slave
- Auto crossover
- 125clk - enabled
- GMII to copper
- Fiber auto-detect - disabled
- Sleep mode - disabled

Ethernet signals from PHY are connected to B2B connector J1. To use Ethernet in your design, GigaBee module should be connected to the carrier board, which have Ethernet magnetics and RJ45 connector. TE0603 carrier board can be used to access Ethernet capabilities of GigaBee XC6SLX series modules.
For correct operation of the Marvell PHY it is required that PHY Reset pin sees valid low level each time power is applied and also during any brownout situations where system Power is removed for short time, but some pins are not at valid logic levels.

Solutions:

1) if GbE PHY is not used PHY reset pin can be tied off to GND
2) if PLL is used from PHY clock, then PLL "locked" output can be used to reset PHY - as long PLL is not locked, it will keep PHY in reset
3) Reset pulse generation circuit clocked from FPGA internal configuration clock, this circuit can force PHY reset pin to low when external clock from PHY is not available
4) any custom Reset circuit that is guaranteed to drive PHY reset to low level at least once after FPGA configuration when PHY clock is not running.
5) any user logic that is guaranteed to drive PHY reset low after FPGA configuration (without using PHY clock).

Explanation: Marvell PHY samples the MODE pins ONLY when it sees low level on PHY reset input, it does not sample those pins during short power off situations (if the reset pin holds high level because of pin capacitance and high impedance of the pins)! So it is possible that the PHY mode is reset, but the mode pins are not sampled again - this yields in mode setting where 125MHz reference clock from PHY is not available.

2.9 Oscillators

The module has one 25 MHz oscillator for Ethernet PHY (U9). Ethernet PHY provides clock multiplication and resulting 125 MHz clock acts as a system and user clock for the FPGA (FPGA input pin AA12).

Note: For correct generation start, PHY should receive reset pulse. Recommended way to do it it's to connect PHY reset signal (ETHERNET_PHY_RST_N) to LOCKED output of corresponding DCM (DCM which use 125 MHz from PHY).

The module also provides the footprint for custom 3.3 V single-ended oscillator (U12) which can be installed as an option (FPGA input pin Y13).

2.10 User LED

The module contains one user active-low LED connected to FPGA output pin T20. To access more LEDs, use a carrier board and drive FPGA signals connected to B2B connectors. As LED connected to FPGA bank with configurable VCCIO to light LED FPGA pin should in '0' (low) state. To disable LED FPGA pin should be in ‘Z’ (High impedance).
2.11 Watchdog

GigaBee XS6LX has a watchdog timer that is periodically triggered by a positive or negative transition of the WDI (watchdog input) line (FPGA pin V9). When the supervising system fails to re-trigger the watchdog circuit within the time-out interval (min 1.1 s, typ 1.6 s, max 2.3 s), the /WDO (watchdog output) line becomes active (low). This event also re-initializes the watchdog timer.

If zero-resistors R2 is not assembled, the watchdog is disabled (alternate assembly).

If zero-resistors R2 is assembled, the watchdog can be enabled (standard assembly). In this case there is still two options:

To **enable** the watchdog, after module power-up, drive the WDI signal to generate at least one transition (no matter positive or negative).

To keep watchdog **disabled**, set WDI FPGA signal output to high-impedance. One way to reach this goal is to leave FPGA pin V9 (label IO_L50N_2) undeclared in user constrains file (UCF) and set “unused IOB pins” to “float” in the Xilinx Project Navigator options, see Fig. 12.

(Project properties > Configuration options > Unused IOB Pins > Float).
In the standard assembly, the /WDO (watchdog output) line is left unconnected\(^3\) and the only possibility to reset the module is by driving the /MR (master reset) line active (low) through pin 18 of connector J2.

In the alternate assembly, the /WDO (watchdog output) line is connected through zero-resistor R3 to /MR (master reset) line.

**If alternate assembly is used, pin 18 of connector J2 must be left unconnected.**

---

### 3 Configuration Options

The FPGA on GigaBee XC6SLX board can be configured by means of the following devices:

- Xilinx download cable (JTAG)
- SPI Flash memory

#### 3.1 JTAG Configuration

The FPGA can be configured through the JTAG interface. JTAG signals are connected to B2B connector J2. When GigaBee XC6SLX board is used with the TE0603 carrier board, the JTAG interface can be accessed via connectors J5 and J6 on the carrier board.

#### 3.2 Flash Configuration

Default configuration option for FPGA is "Master Serial/SPI". The bit-stream for the FPGA is stored in a serial Flash chip (U11). See chapter 2.7 Flash Memory for additional information.

#### 3.3 eFUSE Programming

eFUSE programming feature is not directly supported by GigaBee XC6SLX modules, but it is possible to use it. To program eFUSE, please follow the steps below:

- Connect VCCAUX to 3.3V power rail.
  
  On TE0603 it can be done by connecting J5 pin 2 or J6 “VREF" (VCCAUX) to J1 any pin from 1,2,3,4 (3.3V). See Figure 13.
- Program eFUSE using JTAG cable and iMPACT software.
- Remove power supply connections to VCCAUX

---

\(^3\) Resistor R3 is not populated.
This section describes how the various pins on B2B connectors J1 and J2 connects to TE0600 on-board components. There are five main signal types connected to B2B connectors:

- FPGA users signals;
- FPGA system signals;
- Power signals;
- Ethernet PHY signals;
- Other system signals.

### Table 9: B2B signals count

<table>
<thead>
<tr>
<th>FPGA Bank</th>
<th>Single-ended</th>
<th>Differential</th>
<th>Total</th>
<th>VCCIO</th>
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</thead>
<tbody>
<tr>
<td>Bank 0</td>
<td>1</td>
<td>22</td>
<td>45</td>
<td>VCCIO 0 (3.3 V)</td>
</tr>
<tr>
<td>Bank 1</td>
<td>1</td>
<td>6</td>
<td>13</td>
<td>VCCIO 1 (1.5 V)</td>
</tr>
<tr>
<td>Bank 2</td>
<td>3</td>
<td>21</td>
<td>45</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Bank 3</td>
<td>0</td>
<td>3</td>
<td>6</td>
<td>1.5 V</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>52</td>
<td>109</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 13: eFUSE Powering**

4 B2B Connectors Pin Descriptions
4.1 Pin Labelling

FPGA user signals connected to B2B connectors are characterized by the "B2B_Bx_Lyy_p" naming convention, where:

- B2B defines a "FPGA to B2B" signal type;
- Bx defines the FPGA bank (x = bank number);
- Lyy defines a differential pair or signal number (yy = pair number);
- p defines a differential signal polarity (P = positive, N = negative); single ended signals do not have this field.

Ethernet PHY signals use "PHY_name" naming conversions where "PHY" defines signal type "PHY to B2B" and "name" is PHY signal name.

Remaining signals use custom names.

4.2 Pin Numbering

Note that GigaBee XC6SLX have hermaphroditic B2B connectors. A feature of hermaphroditic connector numbering is that connected signal numbers don't match. Odd signals on module connect to even signals on baseboard. For example module signal 1 to baseboard signal 2, module signal 2 to baseboard signal 1, module signal 3 to baseboard signal 4 and so on.

4.3 Pin Types

Most pins of B2B connectors J1 and J2 are general-purpose, user-defined I/O pins (GPIOs). There are, however, up to 8 different functional types of pins on the TE0600, as outlined in Table 10. In pin-out tables Table 11 and Table 12, the individual pins are colour-coded according to pin type as in Table 10.

<table>
<thead>
<tr>
<th>type</th>
<th>colour code</th>
<th>description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIO4</td>
<td>Unrestricted, general-purpose differential user-I/O pin.</td>
<td></td>
</tr>
<tr>
<td>SIO</td>
<td>Unrestricted, general-purpose user-I/O pin.</td>
<td></td>
</tr>
<tr>
<td>CONFIG</td>
<td>Dedicated configuration signals.</td>
<td></td>
</tr>
<tr>
<td>PWRMGMT</td>
<td>Control and status signals for the power-saving Suspend mode.</td>
<td></td>
</tr>
<tr>
<td>JTAG</td>
<td>Dedicated JTAG signals.</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>Dedicated ground pin. All must be connected.</td>
<td></td>
</tr>
<tr>
<td>TE</td>
<td>Trenz Electronic specific pin type. See the description of each pin in the user manual for additional information on the corresponding signals.</td>
<td></td>
</tr>
<tr>
<td>POW</td>
<td>Power signals.</td>
<td></td>
</tr>
<tr>
<td>SPI</td>
<td>SPI signals.</td>
<td></td>
</tr>
<tr>
<td>PHY</td>
<td>Ethernet PHY signals.</td>
<td></td>
</tr>
</tbody>
</table>

Table 10: TE0600 pin types

Note that some of Spartan-6 I/O types are partially compatible, so pins of compatible types can be used as inputs for signal of other type. For example pins from FPGA bank with 1.5V VCCO (IOSTANDARD = LVCMOS15) can be used as inputs for 1.2V, 1.8V, 2.5V and 3.3V signals.

See “Spartan-6 FPGA SelectIO Resources” page 38 for detailed information.

4 DIO pins can be used as SIO.
4.4 External Bank 2 differential clock connection

TE0600-02 module have optional connection to FPGA bank 2 differential clock input pins. To provide connection from B2B_B2_L41_P signal to Y13 FPGA pin, zero-resistor R69 should be soldered. To provide connection B2B_B2_L41_N signal to AB13 FPGA pin, zero-resistor R81 should be soldered. Note that in this case optional user oscillator U13 can't be used.

4.5 J1 Pin-out

<table>
<thead>
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<th>J1 pin</th>
<th>Net</th>
<th>Type</th>
<th>FPGA pin</th>
<th>Net Length</th>
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<th>Net</th>
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<td>GND</td>
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<td>-</td>
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<td>-</td>
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4.6 J2 Pin-out

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<td>B2B_B0_L4_N</td>
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<td>A6</td>
<td>7.65mm</td>
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<td>6.93mm</td>
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<td>A8</td>
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<td>D8</td>
<td>6.87mm</td>
<td>38</td>
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<td>DIO</td>
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<td>48</td>
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<td>49</td>
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<td>GND</td>
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<td>-</td>
<td>50</td>
<td>GND</td>
<td>GND</td>
<td>-</td>
<td>-</td>
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<td>51</td>
<td>B2B_B0_L36_P</td>
<td>DIO</td>
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<td>6.76mm</td>
<td>52</td>
<td>B2B_B0_L35_N</td>
<td>DIO</td>
<td>A11</td>
<td>8.89mm</td>
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<td>5.87mm</td>
<td>54</td>
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<td>DIO</td>
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<td>D14</td>
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<td>56</td>
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<td>8.74mm</td>
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Table 11: J1 pin-out
### 4.7 Signal Integrity Considerations

Traces of differential signals pairs are routed symmetrically (as symmetric pairs).

Traces of differential signals pairs are NOT routed with equal length. For applications where traces length has to be matched or timing differences have to be compensated, Table 11 and Table 12 list the trace length of I/O signal lines measured from FPGA balls to B2B connector pins.

Traces of differential signals pairs are routed with a differential impedance between the two traces of 100 ohm. Single ended traces are routed with 60 ohm impedance.

An electronic version of these pin-out tables are available for download from the Trenz Electronic support area of the web site.

## 5 Module revisions and assembly variants

Module revision coded by 4 FPGA BR[3:0] pins, which can be read by FPGA firmware. All these pins should be configure to have internal PULLUP.

---

5 Difference in signal lines length is negligible for used signal frequency.
Module revisions and assembly variants

Revision 01
- More powerful regulators for 1.2V and 1.5V rails
- VCCAUX separated from 2.5V power rail
- 128Mbit SPI Flash
- Additional secure 1Kbit EEPROM
- Optional B2B connection to bank 2 differential clock input

Revision 02

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<th>BR3 R19</th>
<th>BR2 P16</th>
<th>BR1 N16</th>
<th>BR0 P17</th>
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<td>0</td>
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### Table 13: Board revisions pin coding

Main differences between 01 and 02 revisions:

- More powerful regulators for 1.2V and 1.5V rails
- VCCAUX separated from 2.5V power rail
- 128Mbit SPI Flash
- Additional secure 1Kbit EEPROM
- Optional B2B connection to bank 2 differential clock input

Module assembly variants coded by 4 zero ohm resistors, connected to FPGA AV[3:0] pins. All these pins should be configured to have internal PULLUP.

<table>
<thead>
<tr>
<th>Signal FPGA pin</th>
<th>AV3 M18</th>
<th>AV2 M17</th>
<th>AV1 V20</th>
<th>AV0 U19</th>
<th>Speed grade</th>
<th>SDRAM</th>
<th>Temp grade</th>
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<tr>
<td>TE0600-02[V</td>
<td>B]</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>2x128MBit</td>
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<tr>
<td>TE0600-02[V</td>
<td>B]I</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>2</td>
<td>2x128MBit</td>
</tr>
<tr>
<td>TE0600-02[V</td>
<td>B]F</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>3</td>
<td>2x128MBit</td>
</tr>
<tr>
<td>TE0600-02[V</td>
<td>B]IF</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>3</td>
<td>2x128MBit</td>
</tr>
<tr>
<td>TE0600-02[V</td>
<td>B]MF</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>2x512MBit</td>
</tr>
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</table>

### Table 14: Assembly variants pin coding
6 Related Materials and References

The following documents provide supplementary information useful with this user manual.

6.1 Data Sheets

- Xilinx DS160: Spartan-6 Family Overview
  This overview outlines the features and product selection of the Spartan®-6 family.

- Xilinx DS162: Spartan-6 FPGA Data Sheet: DC and Switching Characteristics
  This data sheet contains the DC and switching characteristic specifications for the Spartan®-6 family.

- Samtec Razor Beam LSHM series overview.
  http://www.samtec.com/LSHM

- Maxim DS2502-E48 product overview.

- Winbond W25Q128BV product overview.
  http://www.winbond.com/hq/enu/ProductAndSales/ProductLines/FlashMemory/SerialFlash/W25Q128BV.htm

- Maxim DS2432 product page.
  http://www.maximintegrated.com/datasheet/index.mvp/id/2914

6.2 Documentation Archives

- Xilinx Spartan-6 Documentation
  http://www.xilinx.com/support/documentation/spartan-6.htm

- Xilinx Documentation
  http://www.xilinx.com/documentation/
  http://www.xilinx.com/support/documentation/

- Trenz Electronic GigaBee Series Documentation
  http://docs.trenz-electronic.de/Trenz_Electronic/products/TE0600-GigaBee_series/

6.3 User Guides

- Xilinx UG380: Spartan-6 FPGA Configuration User Guide
  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.

- Xilinx UG381: Spartan-6 FPGA SelectIO Resources
6.4 Design and Development Tools

- Xilinx ISE Design Suite
  http://www.xilinx.com/ISE/
  http://www.xilinx.com/tools/designtools.htm

- Xilinx ISE Design Suite (version archive)
  http://www.xilinx.com/download/
  http://www.xilinx.com/support/download/

- Xilinx ISE WebPACK
  http://www.xilinx.com/tools/webpack.htm
  http://www.xilinx.com/webpack/

6.5 Design Resources

- Trenz Electronic GigaBee Design Resources
  http://www.trenz-electronic.de/download/d0/Trenz_Electronic/d1/TE0600-
  GigaBee_series.html

- Trenz Electronic GigaBee Reference Designs
  https://github.com/Trenz-Electronic/
  https://github.com/Trenz-Electronic/TE-EDK-IP/
  https://github.com/Trenz-Electronic/TE060X-GigaBee-Reference-Designs/

6.6 Tutorials

- Xilinx UG695: ISE In-Depth Tutorial
  Chapter 8: Configuration Using iMPACT
  http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/ise_tuto
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<td>application programming interface</td>
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<tr>
<td>B2B</td>
<td>board-to-board</td>
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<tr>
<td>DSP</td>
<td>digital signal processing; digital signal processor</td>
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<tr>
<td>EDK</td>
<td>Embedded Development Kit</td>
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<tr>
<td>IOB</td>
<td>input / output blocks; I/O blocks</td>
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<td>IP</td>
<td>intellectual property</td>
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<td>ISP</td>
<td>In-System Programmability</td>
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<td>OTP</td>
<td>one-time programmable</td>
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<td>PB</td>
<td>push button</td>
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consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.
## Document Change History

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