PCN-20160211 TE0712-01 to TE0712-02 Revision Change

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**Products Affected**

This change affects all Trenz Electronic TE0712 SoMs of the first revision: TE0712-01-*.

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**Changes**

**#1 added pullup on SPI "hold"**

**Type:** Enhancement

**Reason:** Makes SPI accessible in case Quad bit is cleared and HOLD pin is pulled low by on chip pulldown

**Impact:** None

**#2 added Testpoints**

**Type:** Improvement

**Reason:** Improvement of production tests

**Impact:** None

**#3 Routed MII clock pin additionally to FPGA**

**Type:** Enhancement

**Reason:** Allows DDR clock to be different from PHY clock

**Impact:** None
#4 Added Testpoints

**Type:** Layout change

**Reason:** Improve production testing

**Impact:** None

#5 routed one more PLL clock output to FPGA

**Type:** Enhancement

**Reason:** One more clock is available from PLL

**Impact:** None

#6 Added I2C SCL Pullup

**Type:** Enhancement

**Reason:** It allows AXI_I2C to be used without defining on-chip pullup on SCL line

**Impact:** None

Method of Identification

The model code and revision number (e.g. TE0712-01 or TE0720-02) are printed on the top side of the PCB.

Production Shipment Schedule

From March 2016.

Contact Information

If you have any questions related to this PCN, please contact Trenz Electronic's Technical Support at

- forum.trenz-electronic.de
- wiki.trenz-electronic.de
- support%trenz-electronic.de (subject = PCN-20160211)
• phone
  • national calls: 05223 65301-0
  • international calls: 0049 5223 65301-0

Disclaimer

Any projected dates in this PCN are based on the most current product information at the time this PCN is being issued, but they may change due to unforeseen circumstances. For the latest schedule and any other information, please contact your local Trenz Electronic sales office, technical support or local distributor.