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<td>25</td>
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</tr>
<tr>
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<td>26</td>
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<td>26</td>
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<td>26</td>
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<th>Description</th>
<th>Page</th>
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4 Overview

Zynq Design PS with Linux and simple frequency counter to measure MGT Reference CLK with Vivado HW-Manager. Refer to http://trenz.org/te0715-info for the current online version of this manual and other available documentation.

4.1 Key Features

- PetaLinux
- SD
- ETH
- USB
- I2C
- RTC
- FMeter
- SI5338 Initialisation with FSBL (optional)
- Special FSBL for QSPI Programming

4.2 Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Viva do</th>
<th>Project Built</th>
<th>Authors</th>
<th>Description</th>
</tr>
</thead>
</table>
| 2018-10-01| 201 8.2 | TE0715-test_board-vivado_2018.2-build_03_20181001131411.zip                  | John Hartfiel  | • Rework Board Part Files (PS)  
|           |         | TE0715-test_board_noprebuilt-vivado_2018.2-build_03_20181001131421.zip       |                 | • small design changes  
|           |         |                                                                                |                 | • SI5338 reconfiguration default activated on FSBL  
<p>|           |         |                                                                                |                 | • update linux startup app                                                                   |
| 2018-04-26| 201 7.4 | TE0715-test_board-vivado_2017.4-build_07_20180426171530.zip                  | John Hartfiel  | • new assembly variant  |
|           |         | TE0715-test_board_noprebuild-vivado_2017.4-build_07_20180426171546.zip       |                 |                                           |
| 2018-03-27| 201 7.4 | te0715-test_board-vivado_2017.4-build_07_20180327223552.zip                  | John Hartfiel  | • Board Part Bug fix with UART 1 |
|           |         | te0715-test_board_noprebuild-vivado_2017.4-build_07_20180327223606.zip       |                 |                                           |</p>
<table>
<thead>
<tr>
<th>Date</th>
<th>Viva do</th>
<th>Project Built</th>
<th>Author</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018-01-05</td>
<td>201.7.4</td>
<td>te0715-test_board-vivado_2017.4-build_01_20180105195436.zip</td>
<td>John Hartfiel</td>
<td>• No Design changes&lt;br&gt;• Add FSBL for Flash Programming</td>
</tr>
<tr>
<td></td>
<td></td>
<td>te0715-test_board_noprebuilt-vivado_2017.4-build_01_20180105195452.zip</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2017-11-10</td>
<td>201.7.2</td>
<td>te0715-test_board-vivado_2017.2-build_05_20171110134232.zip</td>
<td>John Hartfiel</td>
<td>• New Web Link on Board Part Files&lt;br&gt;• Add optional FSBL Code to reprogram SI5338</td>
</tr>
<tr>
<td></td>
<td></td>
<td>te0715-test_board_noprebuilt-vivado_2017.2-build_05_20171110134247.zip</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2017-10-19</td>
<td>201.7.2</td>
<td>te0715-test_board-vivado_2017.2-build_04_20171019141808.zip</td>
<td>John Hartfiel</td>
<td>• changed Flash typ on TE0715_board_files.csv (older one is not supported on Vivado 2017.2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>te0715-test_board_noprebuilt-vivado_2017.2-build_04_20171019141825.zip</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2017-09-22</td>
<td>201.7.2</td>
<td>te0715-test_board-vivado_2017.2-build_02_20170927143412.zip</td>
<td>John Hartfiel</td>
<td>• initial release</td>
</tr>
<tr>
<td></td>
<td></td>
<td>te0715-test_board_noprebuilt-vivado_2017.2-build_02_20170927143427.zip</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Table 1: Design Revision History**

### 4.3 Release Notes and Know Issues

<table>
<thead>
<tr>
<th>Issues</th>
<th>Description</th>
<th>Workaround</th>
<th>To be fixed version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timing problems with Frequency counter</td>
<td>can be ignored</td>
<td>---</td>
<td>with 2018-10-01 update</td>
</tr>
</tbody>
</table>

**Table 2: Known Issues**

### 4.4 Requirements

#### 4.4.1 Software
<table>
<thead>
<tr>
<th>Software</th>
<th>Version</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vivado</td>
<td>2018.2</td>
<td>needed</td>
</tr>
<tr>
<td>SDK</td>
<td>2018.2</td>
<td>needed</td>
</tr>
<tr>
<td>PetaLinux</td>
<td>2018.2</td>
<td>needed</td>
</tr>
<tr>
<td>SI5338 Clock Builder</td>
<td>---</td>
<td>optional</td>
</tr>
</tbody>
</table>

Table 3: Software

### 4.4.2 Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files).

Complete List is available on `<design name>/board_files/*/board_files.csv`

Design supports following modules:

<table>
<thead>
<tr>
<th>Module Model</th>
<th>Board Part Short Name</th>
<th>PCB Revision Support</th>
<th>DDR</th>
<th>QSPI Flash</th>
<th>Others</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0715-03-1 5-1C</td>
<td>03_15_1c</td>
<td>REV01,02,03</td>
<td>1GB</td>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0715-03-1 5-1I</td>
<td>03_15_1i</td>
<td>REV01,02,03</td>
<td>1GB</td>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0715-03-1 5-2I</td>
<td>03_15_2i</td>
<td>REV01,02,03</td>
<td>1GB</td>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0715-03-3 0-1C</td>
<td>03_30_1c</td>
<td>REV01,02,03</td>
<td>1GB</td>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0715-03-3 0-1I</td>
<td>03_30_1i</td>
<td>REV01,02,03</td>
<td>1GB</td>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0715-03-3 0-3E</td>
<td>03_30_3e</td>
<td>REV01,02,03</td>
<td>1GB</td>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0715-04-1 5-1C</td>
<td>04_15_1c</td>
<td>REV04</td>
<td>1GB</td>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0715-04-1 5-1I</td>
<td>04_15_1i</td>
<td>REV04</td>
<td>1GB</td>
<td>32</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

1. [https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files](https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files)
Table 4: Hardware Modules

Design supports following carriers:

<table>
<thead>
<tr>
<th>Carrier Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0701</td>
<td></td>
</tr>
<tr>
<td>TE0703</td>
<td>used as reference carrier</td>
</tr>
<tr>
<td>TE0705</td>
<td></td>
</tr>
<tr>
<td>TE0706</td>
<td></td>
</tr>
<tr>
<td>TEBA0841</td>
<td></td>
</tr>
</tbody>
</table>

Table 5: Hardware Carrier

Additional HW Requirements:
### Additional Hardware

<table>
<thead>
<tr>
<th>Additional Hardware</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB Cable for JTAG/UART</td>
<td>Check Carrier Board and Programmer for correct type</td>
</tr>
<tr>
<td>XMOD Programmer</td>
<td>Carrier Board dependent, only if carrier has no own FTDI</td>
</tr>
</tbody>
</table>

Table 6: Additional Hardware

### 4.5 Content

For general structure and of the reference design, see [Project Delivery](https://wiki.trenz-electronic.de/display/PD/Project+Delivery)

#### 4.5.1 Design Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vivado</td>
<td><code>&lt;design name&gt;/block_design</code></td>
<td>Vivado Project will be generated by TE Scripts</td>
</tr>
<tr>
<td></td>
<td><code>&lt;design name&gt;/constraints</code></td>
<td></td>
</tr>
<tr>
<td></td>
<td><code>&lt;design name&gt;/ip_lib</code></td>
<td></td>
</tr>
<tr>
<td>SDK/HSI</td>
<td><code>&lt;design name&gt;/sw_lib</code></td>
<td>Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI</td>
</tr>
<tr>
<td>PetaLinux</td>
<td><code>&lt;design name&gt;/os/petalingux</code></td>
<td>PetaLinux template with current configuration</td>
</tr>
</tbody>
</table>

Table 7: Design sources

#### 4.5.2 Additional Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>SI5338</td>
<td><code>&lt;design name&gt;/misc/SI5338</code></td>
<td>SI5345 Project with current PLL Configuration</td>
</tr>
</tbody>
</table>

Table 8: Additional design sources

#### 4.5.3 Prebuilt

---

2 [https://wiki.trenz-electronic.de/display/PD/Project+Delivery](https://wiki.trenz-electronic.de/display/PD/Project+Delivery)
<table>
<thead>
<tr>
<th>File</th>
<th>File-Extension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIF-File</td>
<td>*.bif</td>
<td>File with description to generate Bin-File</td>
</tr>
<tr>
<td>BIN-File</td>
<td>*.bin</td>
<td>Flash Configuration File with Boot-Image (Zynq-FPGAs)</td>
</tr>
<tr>
<td>BIT-File</td>
<td>*.bit</td>
<td>FPGA (PL Part) Configuration File</td>
</tr>
<tr>
<td>DebugProbes-File</td>
<td>*.ltx</td>
<td>Definition File for Vivado/Vivado Labtools Debugging Interface</td>
</tr>
<tr>
<td>Diverse Reports</td>
<td>---</td>
<td>Report files in different formats</td>
</tr>
<tr>
<td>Hardware-Platform-Specification-Files</td>
<td>*.hdf</td>
<td>Exported Vivado Hardware Specification for SDK/HSI and PetaLinux</td>
</tr>
<tr>
<td>LabTools Project-File</td>
<td>*.lpr</td>
<td>Vivado Labtools Project File</td>
</tr>
<tr>
<td>OS-Image</td>
<td>*.ub</td>
<td>Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)</td>
</tr>
<tr>
<td>Software-Application-File</td>
<td>*.elf</td>
<td>Software Application for Zynq or MicroBlaze Processor Systems</td>
</tr>
</tbody>
</table>

Table 9: Prebuilt files (only on ZIP with prebuilt content)

### 4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0715 "Test Board" Reference Design\(^3\)

---

5 Design Flow

Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:
- Vivado/SDK/SDSoC
- Vivado Projects
- Project Delivery

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery

Currently limitations of functionality

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project
   a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
   Note: Select correct one, see TE Board Part Files
5. Create HDF and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
   Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder

---

5 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects
6 https://wiki.trenz-electronic.de/display/PD/Project+Delivery
7 https://wiki.trenz-electronic.de/display/PD/Project+Delivery#ProjectDelivery-Currentlylimitationsoffunctionality
8 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files
6. Create Linux (uboot.elf and image.ub) with exported HDF
   a. HDF is exported to "prebuilt\hardware\<short name>"
      Note: HW Export from Vivado GUI create another path as default workspace.
   b. Create Linux images on VM, see [PetaLinux KICKstart](https://wiki.trenz-electronic.de/display/PD/PetaLinuxKICKstart)
      i. Use TE Template from /os/petalingux
          Note: run init_config.sh before you start petalingux config. This will set correct temporary path variable.

7. Add Linux files (uboot.elf and image.ub) to prebuilt folder
   a. "prebuilt\os\petalingux\default" or "prebuilt\os\petalingux\<short name>"
      Notes: Scripts select "prebuilt\os\petalingux\<short name>", if exist, otherwise "prebuilt\os\petalingux\default"

8. Generate Programming Files with HSI/SDK
   a. Run on Vivado TCL: TE::sw_run_hsi
      Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
   b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk
      Note: See [SDK Projects](https://wiki.trenz-electronic.de/display/PD/SDKProjects)
6 Launch

⚠️ Check Module and Carrier TRMs for proper HW configuration before you try any design.
Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first lunch.
TE0715-0x-30-xx only: HP IO Banks max power supply voltage is 1.8V.

6.1 Programming

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

6.1.1 QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp u-boot
   Note: To program with SDK/Vivado GUI, use special FSBL (zynq_fsbl_flash) on setup
   optional "TE::pr_program_flash_binfile -swapp hello_te0715" possible
4. Copy image.ub on SD-Card
5. Insert SD-Card

6.1.2 SD

1. Copy image.ub and Boot.bin on SD-Card.
   - For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Set Boot Mode to SD-Boot.
   - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

6.1.3 JTAG

Not used on this Example.

6.2 Usage

1. Prepare HW like described on section Programming (see page 14)
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)
   Note: See TRM of the Carrier, which is used.
4. Power On PCB
   Note: 1. Zynq Boot ROM loads FSBL from SD into OCM, 2. FSBL loads U-boot from SD into DDR, 3. U-boot load Linux from SD into DDR

---

6.2.1 Linux

1. Open Serial Console (e.g. putty)
   a. Speed: 115200
   b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Linux Console:
   Note: Wait until Linux boot finished For Linux Login use:
   a. User Name: root
   b. Password: root
3. You can use Linux shell now.
   a. I2C 1 Bus type: i2cdetect -y -r 1
   b. RTC check: dmesg | grep rtc
   c. ETH0 works with udhcpc

6.2.2 Vivado HW Manager

CLK Counters:

1. Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).
   a. Set radix from VIO signals to unsigned integer.
      Note: Frequency Counter is inaccurate and displayed unit is Hz
   b. MGT CLK is configured to 125MHz by default, FCLK is not configured by default (optional possible over FSBL, see FSBL description).

![Vivado Hardware Manager](image)

Figure 1: Vivado Hardware Manager
7 System Design - Vivado

7.1 Block Design

Figure 2: Block Design

7.1.1 PS Interfaces

Activated interfaces:

<table>
<thead>
<tr>
<th>Type</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR</td>
<td>---</td>
</tr>
<tr>
<td>QSPI</td>
<td>MIO</td>
</tr>
<tr>
<td>I2C1</td>
<td>MIO</td>
</tr>
<tr>
<td>UART0</td>
<td>MIO</td>
</tr>
<tr>
<td>GPIO</td>
<td>MIO</td>
</tr>
<tr>
<td>ETH, USB Rst</td>
<td>MIO</td>
</tr>
<tr>
<td>Type</td>
<td>Note</td>
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<td>-----------</td>
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<tr>
<td>SD0</td>
<td>MIO</td>
</tr>
<tr>
<td>USB0</td>
<td>MIO</td>
</tr>
<tr>
<td>ETH0</td>
<td>MIO</td>
</tr>
<tr>
<td>TTC0..1</td>
<td>EMIO</td>
</tr>
<tr>
<td>WDT</td>
<td>EMIO</td>
</tr>
</tbody>
</table>

**Table 10: PS Interfaces**

### 7.2 Constrains

#### 7.2.1 Basic module constrains

_i_bitgen_common.xdc

- set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
- set_property CONFIG_VOLTAGE 3.3 [current_design]
- set_property CFGBVS VCCO [current_design]
- set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]

_i_unused_io.xdc

- set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]

#### 7.2.2 Design specific constrain

_i_io.xdc

- set_property PACKAGE_PIN K2 [get_ports {fclk[0]}]
- set_property IOSTANDARD LVCMOS18 [get_ports {fclk[0]}]
- set_property CLOCKDEDICATED_ROUTE FALSE [get_nets fclk_IBUF[0]]
# for fmeter only
set_false_path -from [get_clocks clk_fpga_0] -to [get_clocks {zsys_i/util_ds_buf_0/U0/IBUF_OUT[0]}]
set_false_path -from [get_clocks {zsys_i/util_ds_buf_0/U0/IBUF_OUT[0]}] -to [get_clocks clk_fpga_0]
set_false_path -from [get_clocks clk_fpga_0] -to [get_clocks {zsys_i/util_ds_buf_1/U0/BUFG_0[0]}]
8 Software Design - SDK/HSI

For SDK project creation, follow instructions from:

- SDK Projects

8.1 Application

Template location: ./sw_lib/sw_apps/

8.1.1 zynq_fsbl

TE modified 2018.2 FSBL

Changes:

- Si5338 Configuration
  - see main.c, fsbl_hooks.c (d/remove define RECONFIGURE_SI5338 to enable PLL programming with given register_map.h setup (default activate))
  - Add register_map.h, si5338.c, si5338.h

8.1.2 zynq_fsbl_flash

TE modified 2018.2 FSBL

Changes:

- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation

8.1.3 hello_te0715

Hello TE0715 is a Xilinx Hello World example as endless loop instead of one console output.

8.1.4 u-boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.

12 https://wiki.trenz-electronic.de/display/PD/SDK+Projects
9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart\(^{13}\)

9.1 Config

No changes.

9.2 U-Boot

No changes.

\(^{13}\)https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart
9.3 Device Tree

```
#include/ "system-conf.dtsi"
/

/ * default */
/ * ETH PHY */
&gem0 {
    status = "okay";
    ethernet_phy0: ethernet-phy0 {
        compatible = "marvell,88e1510";
        device_type = "ethernet-phy";
        reg = <0>;
    }
};

/ * USB PHY */
/
    usb_phy0: usb_phy0 {
        compatible = "ulpi-phy";
        //compatible = "usb-nop-xceiv";
        #phy-cells = <0>;
        reg = <0xe0002000 0x1000>;
        view-port = <0x0170>;
        drv-vbus;
    }
};

&usb0 {
    dr_mode = "host";
    //dr_mode = "peripheral";
    usb-phy = <&usb_phy0>;
};

/ * I2C */
// i2c PLL: 0x70, i2c eeprom: 0x50

&i2c1 {
    rtc@6F { // Real Time Clock
        compatible = "isl12022";
        reg = <0x6F>;
    }
};
```
9.4 Kernel

Activate:
  - RTC_DRV_ISL12022

9.5 Rootfs

Activate:
  - i2c-tools

9.6 Applications

9.6.1 startup

Script App to load init.sh from SD Card if available.
See: \os\petalinux\project-spec\meta-user\recipes-apps\startup\files
10 Additional Software

10.1 SI5338

File location <design name>/misc/SI5338/RegisterMap.txt

General documentation how you work with these project will be available on SI5338

14 https://wiki.trenz-electronic.de/display/PD/SI5338
## 11 Appx. A: Change History and Legal Notices

### 11.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

<table>
<thead>
<tr>
<th>Date</th>
<th>Document Revision</th>
<th>Authors</th>
<th>Description</th>
</tr>
</thead>
</table>
| 2018-10-01 | v. 31(see page 6) | John Hartfiel15 | • Release 2018.2  
  • Redesign Board Part Files  
  • New activate SI5338 example over FSBL  
  • small Design changes  
  • Update Documentation Style  
  • Update in process and will be available soon |
| 2018-04-26 | v.30              | John Hartfiel   | • New assembly variant                                                      |
| 2018-03-27 | v.29              | John Hartfiel   | • Bugfix Board Part Files                                                  |
| 2018-02-13 | v.28              | John Hartfiel   | • Release 2017.4                                                           |
| 2017-11-10 | v.22              | John Hartfiel   | • Design Update with new options  
  • Add SI5338 section  
  • Update FSBL section |
| 2017-10-19 | v.21              | John Hartfiel   | • Download Update                                                           |

15 https://wiki.trenz-electronic.de/display/~j.hartfiel
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11.3 Data privacy

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16 [https://wiki.trenz-electronic.de/display/~j.hartfiel](https://wiki.trenz-electronic.de/display/~j.hartfiel)
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\(^{18}\) [https://echa.europa.eu/candidate-list-table](https://echa.europa.eu/candidate-list-table)
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