TE0720 Test Board
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Overview

Zynq PS Design with Linux Example and PHY status LED on Vivado HW-Manager.

Key Features

- PetaLinux
- SD
- ETH (use EEPROM MAC)
- USB
- I2C
- RTC
- VIO PHY LED
- FSBL for EEPROM MAC and CPLD access
- Special FSBL for QSPI Programming

Revision History

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<th>Vivado</th>
<th>Project Built</th>
<th>Authors</th>
<th>Description</th>
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<td>2018-04-26</td>
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<td>test_board_vivado_2017.4-build_07_20180426144351.zip, test_board_noprebuild-vivado_2017.4-build_07_20180426144405.zip</td>
<td>John Hartfiel</td>
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<td>• no design changes • set EEPROM MAC with FSBL+u-boot • FSBL for QSPI Programming</td>
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Release Notes and Know Issues

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<th>To be fixed version</th>
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## Requirements

### Software

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<td>PetaLinux</td>
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### Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](http://www.trenz-electronic.de).

Complete List is available on `<design name>/board_files/*_board_files.csv`

Design supports following modules:

<table>
<thead>
<tr>
<th>Module Model</th>
<th>Board Part Short Name</th>
<th>PCB Revision Support</th>
<th>DDR</th>
<th>QSPI Flash</th>
<th>Others</th>
<th>Notes</th>
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Design supports following carriers:

<table>
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<td>TE0701</td>
<td>* See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers</td>
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Carrier Model | Notes
---|---
TE0703 | • See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers  
• Used as reference carrier.
TE0705 | • See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers
TE0706 | • See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers
TEBA0841 | • See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers  
• No SD Slot available, pins goes to Pin Header  
• For TEBA0841 REV01, please contact TE support

Additional HW Requirements:

| Additional Hardware | Notes |
---|---
USB Cable for JTAG/UART | Check Carrier Board and Programmer for correct type
XMOD Programmer | Carrier Board dependent, only if carrier has no own FTDI

Content

For general structure and of the reference design, see Project Delivery

Design Sources

| Type | Location | Notes |
---|---|---
Vivado | `<design name>/block_design`  
`<design name>/constraints`  
`<design name>/ip_lib` | Vivado Project will be generated by TE Scripts
SDK/HSI | `<design name>/sw_lib` | Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI
PetaLinux | `<design name>/os/petalinux` | PetaLinux template with current configuration

Additional Sources

| Type | Location | Notes |
---|---|---

Prebuilt

| File | File-Extension | Description |
---|---|---
BIF-File | `.bif` | File with description to generate Bin-File
BIN-File | `.bin` | Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File | `.bit` | FPGA (PL Part) Configuration File
DebugProbes-File | `.ltx` | Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports | --- | Report files in different formats
## Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0720 "Test Board" Reference Design

<table>
<thead>
<tr>
<th>File</th>
<th>File-Extension</th>
<th>Description</th>
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<tbody>
<tr>
<td>Hardware-Platform-Specification-Files</td>
<td>*.hdf</td>
<td>Exported Vivado Hardware Specification for SDK/HSI and PetaLinux</td>
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<tr>
<td>LabTools Project-File</td>
<td>*.lpr</td>
<td>Vivado Labtools Project File</td>
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<tr>
<td>OS-Image</td>
<td>*.ub</td>
<td>Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)</td>
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<tr>
<td>Software-Application-File</td>
<td>*.elf</td>
<td>Software Application for Zynq or MicroBlaze Processor Systems</td>
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</table>
Design Flow

⚠️ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:
- Vivado/SDK/SDSoC\#XilinxSoftware-BasicUserGuides
- Vivado Projects
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with ".create_win_setup.cmd" on Windows OS and ".create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. .create_win_setup.cmd/.create_linux_setup.sh and follow instructions on shell:

2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project
   a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
   Note: Select correct one, see TE Board Part Files
5. Create HDF and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
      Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is
      the same, except file export to prebuilt folder

6. Create Linux (uboot.elf and image.ub) with exported HDF
   a. HDF is exported to "prebuilt\hardware\<short name>"
      Note: HW Export from Vivado GUI create another path as default workspace.
   b. Create Linux images on VM, see PetaLinux KICKstart
      i. Use TE Template from /os/petalinux
         Note: run init_config.sh before you start petalinux config. This will set correct temporary
         path variable.

7. Add Linux files (uboot.elf and image.ub) to prebuilt folder
   a. "prebuilt\os\petalinux\default" or "prebuilt\os\petalinux\<short name>"
      Notes: Scripts select "prebuilt\os\petalinux\<short name>", if exist, otherwise
      "prebuilt\os\petalinux\default"

8. Generate Programming Files with HSI/SDK
   a. Run on Vivado TCL: TE::sw_run_hsi
      Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.
      csv"
   b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::
      sw_run_sdk
      Note: See SDK Projects
Launch

Programming

⚠️ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp u-boot
   Note: To program with SDK/Vivado GUI, use special FSBL (zynq_fsbl_flash) on setup
4. Copy image.ub on SD-Card
5. Insert SD-Card

SD

1. Copy image.ub and Boot.bin on SD-Card.
   • For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Set Boot Mode to SD-Boot.
   • Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

JTAG

Not used on this Example.

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)
   Note: See TRM of the Carrier, which is used.
4. Power On PCB
   Note: 1. Zynq Boot ROM loads FSBL from SD into OCM, 2. FSBL loads U-boot from SD into DDR, 3. U-boot load Linux from SD into DDR
Linux

1. Open Serial Console (e.g. putty)
   a. Speed: 115200
   b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)

2. Linux Console:
   Note: Wait until Linux boot finished For Linux Login use:
   a. User Name: root
   b. Password: root

3. You can use Linux shell now.
   a. I2C 0 Bus type: i2cdetect -y -r 0
   b. I2C 1 Bus type: i2cdetect -y -r 1
   c. RTC check: dmesg | grep rtc
   d. ETH0 works with udhcpc
   e. USB: insert USB device

Vivado HW Manager

1. Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).

2. PHY LED:
System Design - Vivado

Block Design

PS Interfaces

<table>
<thead>
<tr>
<th>Type</th>
<th>Note</th>
</tr>
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<td>DDR</td>
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<tr>
<td>QSPI</td>
<td>MIO</td>
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<td>GPIO</td>
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<tr>
<td>TTC</td>
<td>EMIO</td>
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</table>
Constrains

Basic module constrains

__i_bitgen_common.xdc

# # Common BITGEN related settings for TE0720 SoM
# set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]

__i_common.xdc

# set_property BITSTREAM.CONFIG.UNUSEDPIN PULLUP [current_design]

Design specific constrain

__i_TE0720-SC.xdc

# # Constraints for System controller support logic
# set_property PACKAGE_PIN K16 [get_ports PL_pin_K16]
set_property PACKAGE_PIN K19 [get_ports PL_pin_K19]
set_property PACKAGE_PIN K20 [get_ports PL_pin_K20]
set_property PACKAGE_PIN L16 [get_ports PL_pin_L16]
set_property PACKAGE_PIN M15 [get_ports PL_pin_M15]
set_property PACKAGE_PIN N15 [get_ports PL_pin_N15]
set_property PACKAGE_PIN N22 [get_ports PL_pin_N22]
set_property PACKAGE_PIN P16 [get_ports PL_pin_P16]
set_property PACKAGE_PIN P22 [get_ports PL_pin_P22]

# # If Bank 34 is not 3.3V Powered need change the IOSTANDARD
# set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_P22]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_P16]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_N22]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_N15]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_M15]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_L16]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_K20]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_K19]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_K16]
Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects

Application

FSBL

TE modified 2017.4 FSBL

Functions:

- Read EEPROM MAC Address and make Address accessible by UBOOT (need copy defines on uboot platform-top.h)
- Read CPLD Firmware and SoC Type
- CPLD Interface
- Configure Marvell PHY

Changes:

- Add te_fsbl_config.h, te_fsbl_hooks.h te_fsbl_hooks.c, and includ into fsbl_hooks.c

zynq_fsbl_flash

TE modified 2017.4 FSBL

Changes:

- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation

Hello TE0720

Hello World App in Endless loop.

U-Boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.
Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

Config

- Subsystem Auto Hardware Settings: Serial Settings: ps7_uart_0

U-Boot

```
#include <configs/platform-auto.h>

#define CONFIG_PREBOOT    "echo U-BOOT for petalinux;echo importing env from FSBL shared area at 0xFFFFFC00; if i test "0xFFFFFC00 == 0xCAFEBABE; then echo Found valid magic; env import -t 0xFFFFFC04; fi;setenv preboot; echo; dhcp"
```

Device Tree

```
#include/ "system-conf.dtsi"
/
};

/* default */

/* Flash */
&qspi {
    flash0: flash0 {
        compatible = "w25q256";
    };
};

/* ETH PHY */
&gem0 {
    phy-handle = < phy0>;
    mdio {
        #address-cells = <1>;
        #size-cells = <0>;
        phy0: phy0 {
            compatible = "marvell,88e1510";
            device_type = "ethernet-phy";
            reg = <0>;
        };
    };
};
```
/* USB PHY */

/

   usb_phy0: usb_phy@0 {
      compatible = "ulpi-phy";
      //compatible = "usb-nop-xceiv";
      #phy-cells = <0>
      reg = <0xe0002000 0x1000>
      view-port = <0x0170>
      drv-vbus
   }
};

&usb0 {
   dr_mode = "host";
   //dr_mode = "peripheral"
   usb-phy = <&usb_phy0>
};

/* I2C need I2C1 connected to te0720 system controller ip */
&i2c1 {
   iexp@20 { // GPIO in CPLD
      #gpio-cells = <2>
      compatible = "ti,pcf8574"
      reg = <0x20>
      gpio-controller;
   }

   iexp@21 { // GPIO in CPLD
      #gpio-cells = <2>
      compatible = "ti,pcf8574"
      reg = <0x21>
      gpio-controller;
   }

   rtc@6F { // Real Time Clock
      compatible = "isl12022"
      reg = <0x6F>
   }
};

Kernel
Activate:

   • RTC_DRV_ISL12022

Rootfs
Activate:
• i2c-tools

Applications

startup

Script App to load init.sh from SD Card if available.

See: `/os/petalinux/project-spec/meta-user/recipes-apps/startup/files`
Additional Software

No additional software is needed.
Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to “Change History” of this page and select older document revision number.

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<th>Authors</th>
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<td>John Hartfiel</td>
<td>• add assembly variant</td>
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<td>v.14</td>
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<td>v.12</td>
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<td>• Update HW list</td>
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<td>2017-11-20</td>
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Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.
REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE


Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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