TE0720 Test Board

Revision v.25
Exported on 2019-02-14

Online version of this document:
https://wiki.trenz-electronic.de/display/PD/TE0720+Test+Board
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<td>11.5 Limitation of Liability</td>
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<td>29</td>
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</tbody>
</table>
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Online version of this manual and other related documents can be found at https://wiki.trenz-electronic.de/display/PD/Trenz+Electronic+Documentation
4 Overview

Zynq PS Design with Linux Example and PHY status LED on Vivado HW-Manager.

4.1 Key Features

- PetaLinux
- SD
- ETH (use EEPROM MAC)
- USB
- I2C
- RTC
- VIO PHY LED
- FSBL for EEPROM MAC and CPLD access
- Special FSBL for QSPI Programming

4.2 Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Vivado</th>
<th>Project Built</th>
<th>Authors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018-08-23</td>
<td>2018.2</td>
<td>te0720-test_board-vivado_2018.2-build_03_20180823185142.zip</td>
<td>John Hartfiel</td>
<td>• DDR setup bugfix for l1if only</td>
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<tr>
<td></td>
<td></td>
<td>te0720-test_board_noprebuild-vivado_2018.2-build_03_20180823185158.zip</td>
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<td></td>
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<td></td>
<td></td>
<td>te0720-test_board_noprebuild-vivado_2018.2-build_02_20180810162040.zip</td>
<td></td>
<td>• Boart Part Files rework</td>
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<tr>
<td>Date</td>
<td>Vivado</td>
<td>Project Built</td>
<td>Authors</td>
<td>Description</td>
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<td>-------------------------------------------------------------------------------</td>
<td>------------</td>
<td>------------------------------------------------------------------</td>
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<tr>
<td>2018-04-26</td>
<td>2017.4</td>
<td>te0720-test_board-vivado_2017.4-build_07_20180426144351.zip</td>
<td>John</td>
<td>• new assembly variant</td>
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<tr>
<td></td>
<td></td>
<td>te0720-test_board_noprebuilt-vivado_2017.4-build_07_20180426144405.zip</td>
<td>Hartfiel</td>
<td></td>
</tr>
<tr>
<td>2018-03-12</td>
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<td>te0720-test_board-noprebuild-vivado_2017.4-build_06_20180312152419.zip</td>
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<td>• script update</td>
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<td>te0720-test_board_noprebuild-vivado_2017.4-build_02_20180109121313.zip</td>
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<td>te0720-test_board-vivado_2017.4-build_02_20180109121300.zip</td>
<td>Hartfiel</td>
<td>• set EEPROM MAC with FSBL+u-boot</td>
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<td></td>
<td></td>
<td>• FSBL for QSPI Programming</td>
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<td>2017-11-27</td>
<td>2017.2</td>
<td>te0720-test_board_noprebuild-vivado_2017.2-build_05_20171127153028.zip</td>
<td>John</td>
<td>• remove duplicated content</td>
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### 4.3 Release Notes and Know Issues

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<th>Issues</th>
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<th>Workaround</th>
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<td>No known issues</td>
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### 4.4 Requirements

#### 4.4.1 Software

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<th>Version</th>
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<td>SDK</td>
<td>2018.2</td>
<td>needed</td>
</tr>
<tr>
<td>PetaLinux</td>
<td>2018.2</td>
<td>needed</td>
</tr>
</tbody>
</table>

#### 4.4.2 Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files).

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

---

1. [https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files](https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files)
<table>
<thead>
<tr>
<th>Module Model</th>
<th>Board Part Short Name</th>
<th>PCB Revision Support</th>
<th>DDR</th>
<th>QSPI Flash</th>
<th>Others</th>
<th>Notes</th>
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<tr>
<td>te0720-03-2if</td>
<td>2if</td>
<td>REV02, REV03</td>
<td>1GB</td>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>te0720-03-2ifc3</td>
<td>2if</td>
<td>REV02, REV03</td>
<td>1GB</td>
<td>32</td>
<td></td>
<td>2.5 mm connector</td>
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<tr>
<td>te0720-03-2ifc8</td>
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<td>REV02, REV03</td>
<td>1GB</td>
<td>32</td>
<td></td>
<td>32GB eMMC</td>
</tr>
<tr>
<td>te0720-03-1qf</td>
<td>1qf</td>
<td>REV02, REV03</td>
<td>1GB</td>
<td>32</td>
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</tr>
<tr>
<td>te0720-03-1qfa</td>
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<td>REV03</td>
<td>1GB</td>
<td>32</td>
<td></td>
<td>Micron instead of Spansion Flash</td>
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<tr>
<td>te0720-03-1cf</td>
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<td></td>
<td>8GB eMMC</td>
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<tr>
<td>te0720-03-2ef</td>
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<td>1GB</td>
<td>32</td>
<td></td>
<td></td>
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<tr>
<td>te0720-03-1cr</td>
<td>1cr</td>
<td>REV02, REV03</td>
<td>256MB</td>
<td>32</td>
<td></td>
<td>without eMMC</td>
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<tr>
<td>te0720-03-l1if</td>
<td>l1if</td>
<td>REV02, REV03</td>
<td>512MB</td>
<td>32</td>
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<td>te0720-03-14s-1c</td>
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<td>REV02, REV03</td>
<td>1GB</td>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>te0720-03-2ifa</td>
<td>2if</td>
<td>REV03</td>
<td>1GB</td>
<td>32</td>
<td></td>
<td>Micron instead of Spansion Flash</td>
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</table>

Design supports following carriers:
### Carrier Model

<table>
<thead>
<tr>
<th>Carrier Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0701</td>
<td>• See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
</tbody>
</table>
| TE0703        | • See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers<sup>3</sup>  
• Used as reference carrier. |
| TE0705        | • See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers<sup>4</sup> |
| TE0706        | • See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers<sup>5</sup> |
| TEBA0841      | • See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers<sup>6</sup>  
• No SD Slot available, pins goes to Pin Header  
• For TEBA0841 REV01, please contact TE support |

### Additional Hardware

<table>
<thead>
<tr>
<th>Additional Hardware</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB Cable for JTAG/UART</td>
<td>Check Carrier Board and Programmer for correct type</td>
</tr>
<tr>
<td>XMOD Programmer</td>
<td>Carrier Board dependent, only if carrier has no own FTDI</td>
</tr>
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</table>

### 4.5 Content

For general structure and of the reference design, see [Project Delivery]<sup>7</sup>

#### 4.5.1 Design Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
</table>
| Vivado     | <design name>/block_design  
<design name>/constraints  
<design name>/ip_lib | Vivado Project will be generated by TE Scripts |
| SDK/HSI    | <design name>/sw_lib | Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI |

---

<sup>2</sup> https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers  
<sup>3</sup> https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers  
<sup>4</sup> https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers  
<sup>5</sup> https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers  
<sup>6</sup> https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers  
<sup>7</sup> https://wiki.trenz-electronic.de/display/PD/Project+Delivery
### 4.5.2 Additional Sources

<table>
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<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>PetaLinux</td>
<td>&lt;design name&gt;/os/petalinux</td>
<td>PetaLinux template with current configuration</td>
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### 4.5.3 Prebuilt

<table>
<thead>
<tr>
<th>File</th>
<th>File-Extension</th>
<th>Description</th>
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<tbody>
<tr>
<td>BIF-File</td>
<td>*.bif</td>
<td>File with description to generate Bin-File</td>
</tr>
<tr>
<td>BIN-File</td>
<td>*.bin</td>
<td>Flash Configuration File with Boot-Image (Zynq-FPGAs)</td>
</tr>
<tr>
<td>BIT-File</td>
<td>*.bit</td>
<td>FPGA (PL Part) Configuration File</td>
</tr>
<tr>
<td>DebugProbes-File</td>
<td>*.ltx</td>
<td>Definition File for Vivado/Vivado Labtools Debugging Interface</td>
</tr>
<tr>
<td>Diverse Reports</td>
<td>---</td>
<td>Report files in different formats</td>
</tr>
<tr>
<td>Hardware-Platform-Specification-Files</td>
<td>*.hdf</td>
<td>Exported Vivado Hardware Specification for SDK/HSI and PetaLinux</td>
</tr>
<tr>
<td>LabTools Project-File</td>
<td>*.lpr</td>
<td>Vivado Labtools Project File</td>
</tr>
<tr>
<td>OS-Image</td>
<td>*.ub</td>
<td>Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)</td>
</tr>
<tr>
<td>Software-Application-File</td>
<td>*.elf</td>
<td>Software Application for Zynq or MicroBlaze Processor Systems</td>
</tr>
</tbody>
</table>

### 4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.
Reference Design is available on:

- **TE0720 "Test Board" Reference Design**

5 Design Flow

Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:
- Vivado/SDK/SDSoC
- Vivado Projects
- Project Delivery

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also be executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery: Currently limitations of functionality.

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project
   a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
   Note: Select correct one, see TE Board Part Files
5. Create HDF and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
      Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (uboot.elf and image.ub) with exported HDF

---

10 https://wiki.trenz-electronic.de/display/PD/VivadoProjects
11 https://wiki.trenz-electronic.de/display/PD/ProjectDelivery
12 https://wiki.trenz-electronic.de/display/PD/ProjectDelivery#ProjectDelivery-Currentlylimitationsoffunctionality
13 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files
a. HDF is exported to "prebuilt\hardware\<short name>"
   Note: HW Export from Vivado GUI create another path as default workspace.
Create Linux images on VM, see PetaLinux KICKstart
   i. Use TE Template from /os/petalinux
      Note: run init_config.sh before you start petalinux config. This will set correct temporary path variable.
7. Add Linux files (uboot.elf and image.ub) to prebuilt folder
   a. "prebuilt\os\petalinux\default" or "prebuilt\os\petalinux\<short name>"
      Notes: Scripts select "prebuilt\os\petalinux\<short name>", if exist, otherwise "prebuilt\os\petalinux\default"
8. Generate Programming Files with HSI/SDK
   a. Run on Vivado TCL: TE::sw_run_hsi
      Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
   b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk
      Note: See SDK Projects

14 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart
15 https://wiki.trenz-electronic.de/display/PD/SDK+Projects
6 Launch

6.1 Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

6.1.1 QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp u-boot
   Note: To program with SDK/Vivado GUI, use special FSBL (zynq_fsbl_flash) on setup
   optional "TE::pr_program_flash_binfile -swapp hello_te0720" possible
4. Copy image.ub on SD-Card
5. Insert SD-Card

6.1.2 SD

1. Copy image.ub and Boot.bin on SD-Card.
   • For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Set Boot Mode to SD-Boot.
   • Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

6.1.3 JTAG

Not used on this Example.

6.2 Usage

1. Prepare HW like described on section Programming (see page 16)
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)
   Note: See TRM of the Carrier, which is used.
4. Power On PCB
   Note: 1. Zynq Boot ROM loads FSBL from SD into OCM, 2. FSBL loads U-boot from SD into DDR, 3. U-boot load Linux from SD into DDR

6.2.1 Linux

1. Open Serial Console (e.g. putty)
   a. Speed: 115200
   b. COM Port: Win OS, see device manager, Linux OS see `dmesg |grep tty` (UART is *USB1)
2. Linux Console:
   Note: Wait until Linux boot finished For Linux Login use:
   a. User Name: root
   b. Password: root
3. You can use Linux shell now.
   a. I2C 0 Bus type: `i2cdetect -y -r 0`
   b. I2C 1 Bus type: `i2cdetect -y -r 1`
   c. RTC check: `dmesg | grep rtc`
   d. ETH0 works with udhcpc
   e. USB: insert USB device

6.2.2 Vivado HW Manager

1. Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).
2. PHY LED:
7 System Design - Vivado

7.1 Block Design

7.1.1 PS Interfaces

<table>
<thead>
<tr>
<th>Type</th>
<th>Note</th>
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<td>QSPI</td>
<td>MIO</td>
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<tr>
<td>I2C1</td>
<td>EMIO</td>
</tr>
</tbody>
</table>
## 7.2 Constrains

### 7.2.1 Basic module constrains

### _i_bitgen_common.xdc

```bash
# # Common BITGEN related settings for TE0720 SoM
#
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
```

### _i_common.xdc

```bash
# set_property BITSTREAM.CONFIG.UNUSEDPIN PULLUP [current_design]
```
7.2.2 Design specific constrain

/_i_TE0720-SC.xdc

# Constraints for System controller support logic
#
set_property PACKAGE_PIN K16 [get_ports PL_pin_K16]
set_property PACKAGE_PIN K19 [get_ports PL_pin_K19]
set_property PACKAGE_PIN K20 [get_ports PL_pin_K20]
set_property PACKAGE_PIN L16 [get_ports PL_pin_L16]
set_property PACKAGE_PIN M15 [get_ports PL_pin_M15]
set_property PACKAGE_PIN N15 [get_ports PL_pin_N15]
set_property PACKAGE_PIN N22 [get_ports PL_pin_N22]
set_property PACKAGE_PIN P16 [get_ports PL_pin_P16]
set_property PACKAGE_PIN P22 [get_ports PL_pin_P22]

# If Bank 34 is not 3.3V Powered need change the IOSTANDARD
#
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_P22]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_P16]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_N22]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_N15]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_M15]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_L16]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_K20]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_K19]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_K16]
8 Software Design - SDK/HSI

For SDK project creation, follow instructions from:
SDK Projects

8.1 Application

Template location: ./sw_lib/sw_apps/

8.1.1 zynq_fsbl

TE modified 2018.2 FSBL

Functions:
- Read EEPROM MAC Address and make Address accessible by UBOOT (need copy defines on uboot platform-top.h)
- Read CPLD Firmware and SoC Type
- CPLD Interface
- Configure Marvell PHY

Changes:
- Add te_fsbl_config.h, te_fsbl_hooks.h te_fsbl_hooks.c, and includ into fsbl_hooks.c

8.1.2 zynq_fsbl_flash

TE modified 2018.2 FSBL

Changes:
- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation

8.1.3 hello_te0720

Hello World App in Endless loop.

8.1.4 u-boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.

17 https://wiki.trenz-electronic.de/display/PD/SDK+Projects
9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

9.1 Config

- Subsystem Auto Hardware Settings: Serial Settings: ps7_uart_0
9.2 U-Boot

```c
#include <configs/platform-auto.h>
#define CONFIG_SYS_BOOTH_LEN 0xF000000
#define DFU_ALT_INFO_RAM "
  "dfu_ram_info=" 
  "setenv dfu_alt_info " 
  "image_ub ram $netstart 0xe000000\0" 
  "dfu_ram=run dfu_ram_info && dfu 0 ram 0\0" 
  "thor_ram=run dfu_ram_info && thordown 0 ram 0\0"

#define DFU_ALT_INFO_MMC "
  "dfu_mmc_info=" 
  "set dfu_alt_info " 
  "${kernel_image} fat 0 1\\;" 
  "dfu_mmc=run dfu_mmc_info && dfu 0 mmc 0\0" 
  "thor_mmc=run dfu_mmc_info && thordown 0 mmc 0\0"

/*Required for uartless designs*/
#ifndef CONFIG_BAUDRATE
#define CONFIG_BAUDRATE 115200
#endif

/*Define CONFIG_ZYNQ_EEPROM here and its necessaries in u-boot menuconfig if you had EEPROM memory. */
#ifndef CONFIG_ZYNQ_EEPROM
#define CONFIG_SYS_I2C_EEPROM_ADDR_LEN 1
#define CONFIG_SYS_I2C_EEPROM_ADDR 0x54
#define CONFIG_SYS_EEPROM_PAGE_WRITE_BITS 4
#define CONFIG_SYS_EEPROM_PAGE_WRITE_DELAY_MS 5
#define CONFIG_SYS_EEPROM_SIZE 1024 /* Bytes */
#define CONFIG_SYS_I2C_MUX_ADDR 0x74
#define CONFIG_SYS_I2C_MUX_EEPROM_SEL 0x4
#endif

#define CONFIG_PREBOOT "echo U-BOOT for petalinux;echo importing env from FSBL shared area at 0xFFFFFC00; if itest *0xFFFFFC00 == 0xCAFEBABE; then echo Found valid magic; env import -t 0xFFFFFC04; fi; setenv preboot; echo; dhcpp"
```
9.3 Device Tree

```c
#include/ "system-conf.dtsi"
/
/ {
/ }
/

/* default */
/* QSPI PHY */
&qspi {
    #address-cells = <1>
    #size-cells = <0>
    status = "okay"
    flash0: flash0 {
        compatible = "jedec,spi-nor"
        reg = <0x0>
        #address-cells = <1>
        #size-cells = <1>
    }
};

/* ETH PHY */
&gem0 {
    phy-handle = <&phy0>
    mdio {
        #address-cells = <1>
        #size-cells = <0>
        phy0: phy0 {
            compatible = "marvell,88e1510"
            device_type = "ethernet-phy"
            reg = <0>
        }
    }
};

/* USB PHY */
/
/
    usb_phy0: usb_phy0 {
        compatible = "ulpi-phy"
        //compatible = "usb-nop-xceiv"
        #phy-cells = <0>
        reg = <0xe0002000 0x1000>
        view-port = <0x0170>
        drv-vbus;
    }
};
&usb0 {
    dr_mode = "host"
    //dr_mode = "peripheral";
```
```c
usb-phy = <&usb_phy0>;
}

/* I2C need I2C1 connected to te0720 system controller ip */
&i2c1 {
    iexp@20 {
        // GPIO in CPLD
        #gpio-cells = <2>
        compatible = "ti,pcf8574"
        reg = <0x20>
        gpio-controller
    }
    iexp@21 {
        // GPIO in CPLD
        #gpio-cells = <2>
        compatible = "ti,pcf8574"
        reg = <0x21>
        gpio-controller
    }
    rtc@6F {
        // Real Time Clock
        compatible = "isl12022"
        reg = <0x6F>
    }
}
```

9.4 Kernel

Activate:
- RTC_DRV_ISL12022

9.5 Rootfs

Activate:
- i2c-tools

9.6 Applications

9.6.1 startup

Script App to load init.sh from SD Card if available.
See: \os\petalinux\project-spec\meta-user\recipes-apps\startup\files
10 Additional Software

No additional software is needed.
# 11 Appx. A: Change History and Legal Notices

## 11.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

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<td>2018-08-30</td>
<td>v.25 (see page 6)</td>
<td>John Hartfiel</td>
<td>• update documentation PS configuration</td>
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<tr>
<td>23.08.2018</td>
<td>v.24</td>
<td>John Hartfiel</td>
<td>• update l1if board parts</td>
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<tr>
<td>13.08.2018</td>
<td>v.23</td>
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<td>26.04.2018</td>
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<td>• add assembly variant</td>
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<td>• Design Files update</td>
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<td>John Hartfiel</td>
<td>• Update HW list</td>
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<td>v.11</td>
<td>John Hartfiel</td>
<td>• Release 2017.2</td>
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<td>2017-11-20</td>
<td>v.1</td>
<td>John Hartfiel</td>
<td>• Initial release</td>
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<td>John Hartfiel</td>
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11.2 Legal Notices

11.3 Data privacy

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\(^3^1\) [https://echa.europa.eu/candidate-list-table](https://echa.europa.eu/candidate-list-table)