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<th>Page</th>
</tr>
</thead>
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<td>12</td>
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<td>29</td>
</tr>
</tbody>
</table>
4 Overview

Zynq PS Design with Linux Example and PHY status LED on Vivado HW-Manager.

Refer to http://trenz.org/te0720-info for the current online version of this manual and other available documentation.

4.1 Key Features

- Vivado 2018.3
- PetaLinux
- SD
- ETH (use EEPROM MAC)
- USB
- I2C
- RTC
- VIO PHY LED
- FSBL for EEPROM MAC and CPLD access
- Special FSBL for QSPI Programming

4.2 Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Vivado</th>
<th>Project Built</th>
<th>Authors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2019-03-04</td>
<td>2018.3</td>
<td>TE0720-test_board-vivado_2018.3-build_01_20190304100745.zip</td>
<td>John Hartfiel</td>
<td>update for -1CR version only (256MB DDR3)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0720-test_board_noprebuilt-vivado_2018.3-build_01_20190304100755.zip</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0720-test_board_noprebuilt-vivado_2018.3-build_01_20190221125133.zip</td>
<td></td>
<td>rework of the FSBLs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>some additional Linux features</td>
</tr>
<tr>
<td>Date</td>
<td>Vivado</td>
<td>Project Built</td>
<td>Authors</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>--------</td>
<td>--------------------------------------------------------------------------------</td>
<td>-----------------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>2018-08-23</td>
<td>2018.2</td>
<td>te0720-test_board-vivado_2018.2-build_03_20180823185142.zip</td>
<td>John Hartfiel</td>
<td>• DDR setup bugfix for l1if only</td>
</tr>
<tr>
<td></td>
<td></td>
<td>te0720-test_board_noprebuilt-vivado_2018.2-build_03_20180823185158.zip</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>te0720-test_board_noprebuilt-vivado_2018.2-build_02_20180810162040.zip</td>
<td></td>
<td>• Boart Part Files rework</td>
</tr>
<tr>
<td>2018-04-26</td>
<td>2017.4</td>
<td>te0720-test_board-vivado_2017.4-build_07_20180426144351.zip</td>
<td>John Hartfiel</td>
<td>• new assembly variant</td>
</tr>
<tr>
<td></td>
<td></td>
<td>te0720-test_board_noprebuilt-vivado_2017.4-build_07_20180426144405.zip</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2018-03-12</td>
<td>2017.4</td>
<td>te0720-test_board_noprebuilt-vivado_2017.4-build_06_20180312152408.zip</td>
<td>John Hartfiel</td>
<td>• add assembly variant</td>
</tr>
<tr>
<td></td>
<td></td>
<td>te0720-test_board-vivado_2017.4-build_06_20180312152419.zip</td>
<td></td>
<td>• script update</td>
</tr>
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</table>
### Table 1: Design Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Vivado</th>
<th>Project Built</th>
<th>Authors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018-01-09</td>
<td>2017.4</td>
<td>te0720-test_board_noprebuilt-vivado_2017.4-build_02_201801091213 13.zip</td>
<td>John Hartfiel</td>
<td>• no design changes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>te0720-test_board_noprebuilt-vivado_2017.4-build_02_201801091213 00.zip</td>
<td></td>
<td>• set EEPROM MAC with FSBL+u-boot</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• FSBL for QSPI Programming</td>
</tr>
<tr>
<td>2017-11-27</td>
<td>2017.2</td>
<td>te0720-test_board_noprebuilt-vivado_2017.2-build_05_201711271530 28.zip</td>
<td>John Hartfiel</td>
<td>• remove duplicated content</td>
</tr>
<tr>
<td></td>
<td></td>
<td>te0720-test_board_noprebuilt-vivado_2017.2-build_05_201711271530 06.zip</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2017-11-20</td>
<td>2017.2</td>
<td>te0720-test_board_noprebuilt-vivado_2017.2-build_05_201711220747 01.zip</td>
<td>John Hartfiel</td>
<td>• initial release</td>
</tr>
<tr>
<td></td>
<td></td>
<td>te0720-test_board_noprebuilt-vivado_2017.2-build_05_201711220746 46.zip</td>
<td></td>
<td></td>
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</tbody>
</table>

#### 4.3 Release Notes and Known Issues

<table>
<thead>
<tr>
<th>Issues</th>
<th>Description</th>
<th>Workaround</th>
<th>To be fixed version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Variant with 256MB DDR only (TE0720-03-1CR)</td>
<td>wrong netboot offset</td>
<td>recreate u-boot on petalinux only</td>
<td>solved with 2019-03-04 update</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 2: Known Issues
4.4 Requirements

4.4.1 Software

<table>
<thead>
<tr>
<th>Software</th>
<th>Version</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vivado</td>
<td>2018.3</td>
<td>needed</td>
</tr>
<tr>
<td>SDK</td>
<td>2018.3</td>
<td>needed</td>
</tr>
<tr>
<td>PetaLinux</td>
<td>2018.3</td>
<td>needed</td>
</tr>
</tbody>
</table>

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.¹
Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

<table>
<thead>
<tr>
<th>Module Model</th>
<th>Board Part Short Name</th>
<th>PCB Revision Support</th>
<th>DDR</th>
<th>QSPI Flash</th>
<th>EMMC</th>
<th>Others</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0720-03-2IF</td>
<td>2if_1gb</td>
<td>REV03</td>
<td>REV02</td>
<td>1GB</td>
<td>32MB</td>
<td>4GB</td>
<td>NA</td>
</tr>
<tr>
<td>TE0720-03-2IFC3</td>
<td>2if_1gb</td>
<td>REV03</td>
<td>REV02</td>
<td>1GB</td>
<td>32MB</td>
<td>4GB</td>
<td>2.5 mm connectors</td>
</tr>
<tr>
<td>TE0720-03-2IFC8</td>
<td>2if_1gb</td>
<td>REV03</td>
<td>REV02</td>
<td>1GB</td>
<td>32MB</td>
<td>32GB</td>
<td>NA</td>
</tr>
<tr>
<td>TE0720-03-1QF</td>
<td>1qf_1gb</td>
<td>REV03</td>
<td>REV02</td>
<td>1GB</td>
<td>32MB</td>
<td>4GB</td>
<td>NA</td>
</tr>
<tr>
<td>TE0720-03-1CF</td>
<td>1cf_1gb</td>
<td>REV03</td>
<td>REV02</td>
<td>1GB</td>
<td>32MB</td>
<td>4GB</td>
<td>NA</td>
</tr>
</tbody>
</table>

¹ https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files
<table>
<thead>
<tr>
<th>Module Model</th>
<th>Board Part Short Name</th>
<th>PCB Revision Support</th>
<th>DDR</th>
<th>QSPI Flash</th>
<th>EMMC</th>
<th>Others</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0720-03-1CFA</td>
<td>1cf_1gb</td>
<td>REV03</td>
<td>REV02</td>
<td>1GB</td>
<td>32MB</td>
<td>8GB</td>
<td>NA</td>
</tr>
<tr>
<td>TE0720-03-2EF</td>
<td>2ef_1gb</td>
<td>REV03</td>
<td>REV02</td>
<td>1GB</td>
<td>32MB</td>
<td>4GB</td>
<td>NA</td>
</tr>
<tr>
<td>TE0720-03-1CR</td>
<td>1cr_256mb</td>
<td>REV03</td>
<td>REV02</td>
<td>256 MB</td>
<td>32MB</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>TE0720-03-1L1F</td>
<td>l1if_512mb</td>
<td>REV03</td>
<td>REV02</td>
<td>512 MB</td>
<td>32MB</td>
<td>4GB</td>
<td>NA</td>
</tr>
<tr>
<td>TE0720-03-14S-1C</td>
<td>14s_1gb</td>
<td>REV03</td>
<td>REV02</td>
<td>1GB</td>
<td>32MB</td>
<td>4GB</td>
<td>NA</td>
</tr>
<tr>
<td>TE0720-03-1QFA</td>
<td>1qf_1gb</td>
<td>REV03</td>
<td>REV02</td>
<td>1GB</td>
<td>32MB</td>
<td>4GB</td>
<td>NA</td>
</tr>
<tr>
<td>TE0720-03-2IFA</td>
<td>2if_1gb</td>
<td>REV03</td>
<td>REV02</td>
<td>1GB</td>
<td>32MB</td>
<td>4GB</td>
<td>NA</td>
</tr>
<tr>
<td>TE0720-03-1QFL</td>
<td>1qf_1gb</td>
<td>REV03</td>
<td>REV02</td>
<td>1GB</td>
<td>32MB</td>
<td>4GB</td>
<td>2.5 mm connector s</td>
</tr>
</tbody>
</table>

**Table 4: Hardware Modules**

Design supports following carriers:

<table>
<thead>
<tr>
<th>Carrier Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0701</td>
<td>• See restrictions on usage with 7 Series Carriers: <a href="https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers">4 x 5 SoM Carriers</a>²</td>
</tr>
</tbody>
</table>
| TE0703 | • See restrictions on usage with 7 Series Carriers: [4 x 5 SoM Carriers](https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers)³  
• Used as reference carrier. |
| TE0705 | • See restrictions on usage with 7 Series Carriers: [4 x 5 SoM Carriers](https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers)⁴ |

² [4 x 5 SoM Carriers](https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers)
³ [4 x 5 SoM Carriers](https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers)
⁴ [4 x 5 SoM Carriers](https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers)
<table>
<thead>
<tr>
<th>Carrier Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0706</td>
<td>• See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers(^5)</td>
</tr>
</tbody>
</table>
| TEBA0841      | • See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers\(^5\)  
• No SD Slot available, pins go to Pin Header  
• For TEBA0841 REV01, please contact TE support |

**Table 5: Hardware Carrier**

Additional HW Requirements:

<table>
<thead>
<tr>
<th>Additional Hardware</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB Cable for JTAG/UART</td>
<td>Check Carrier Board and Programmer for correct type</td>
</tr>
<tr>
<td>XMOD Programmer</td>
<td>Carrier Board dependent, only if carrier has no own FTDI</td>
</tr>
</tbody>
</table>

**Table 6: Additional Hardware**

### 4.5 Content

For general structure and of the reference design, see [Project Delivery - Xilinx devices]\(^7\)

#### 4.5.1 Design Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
</table>
| Vivado | `<design name>/block_design`  
          `<design name>/constraints`  
          `<design name>/ip_lib`  | Vivado Project will be generated by TE Scripts |
| SDK/HSI| `<design name>/sw_lib`  | Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI |
| PetaLinux  | `<design name>/os/petalinux`  | PetaLinux template with current configuration |

**Table 7: Design sources**

---

\(^5\) [https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers](https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers)  
\(^6\) [https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers](https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers)  
\(^7\) [https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices](https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices)
4.5.2 Additional Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>init.sh</td>
<td>&lt;design name&gt;/sd/</td>
<td>Additional Initialization Script for Linux</td>
</tr>
</tbody>
</table>

Table 8: Additional design sources

4.5.3 Prebuilt

<table>
<thead>
<tr>
<th>File</th>
<th>File-Extension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIF-File</td>
<td>*.bif</td>
<td>File with description to generate Bin-File</td>
</tr>
<tr>
<td>BIT-File</td>
<td>*.bit</td>
<td>FPGA (PL Part) Configuration File</td>
</tr>
<tr>
<td>DebugProbes-File</td>
<td>*.ltx</td>
<td>Definition File for Vivado/Vivado Labtools Debugging Interface</td>
</tr>
<tr>
<td>Debian SD-Image</td>
<td>*.img</td>
<td>Debian Image for SD-Card</td>
</tr>
<tr>
<td>Diverse Reports</td>
<td>---</td>
<td>Report files in different formats</td>
</tr>
<tr>
<td>Hardware-Platform-</td>
<td>*.hdf</td>
<td>Exported Vivado Hardware Specification for SDK/HSI and PetaLinux</td>
</tr>
<tr>
<td>Specification-Files</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LabTools Project-File</td>
<td>*.lpr</td>
<td>Vivado Labtools Project File</td>
</tr>
<tr>
<td>OS-Image</td>
<td>*.ub</td>
<td>Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)</td>
</tr>
<tr>
<td>Software-Application-File</td>
<td>*.elf</td>
<td>Software Application for Zynq or MicroBlaze Processor Systems</td>
</tr>
</tbody>
</table>

Table 9: Prebuilt files (only on ZIP with prebuilt content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:
• TE0720 "Test Board" Reference Design
5 Design Flow

![Warning Icon] Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- Xilinx Development Tools
- Vivado Projects - TE Reference Design
- Project Delivery

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with ".\create_win_setup.cmd" on Windows OS and ".\create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery

Currently limitations of functionality

1. .\create_win_setup.cmd/.\create_linux_setup.sh and follow instructions on shell:

   1. Press 0 and enter to start "Module Selection Guide"
   2. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
   3. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process
      a. (optional for manual changes) Select correct device and Xilinx install path on 
         "design_basic_settings.cmd" and create Vivado project with "vivado\_create\_project\_guimode.cmd"
         Note: Select correct one, see TE Board Part Files
   4. Create HDF and export to prebuilt folder
      a. Run on Vivado TCL: TE::hw\_build\_design -export\_prebuilt
         Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder

10 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects-->+TE+Reference+Design
11 https://wiki.trenz-electronic.de/display/PD/Project+Delivery-->+Xilinx+devices
12 https://wiki.trenz-electronic.de/display/PD/Project+Delivery-->+Xilinx+devices#ProjectDelivery-Xilinxdevices-Currentlylimitationsoffunctionality
13 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files
6. Create Linux (uboot.elf and image.ub) with exported HDF
   a. HDF is exported to "prebuilt\hardware\<short name>"
      Note: HW Export from Vivado GUI create another path as default workspace.
      Create Linux images on VM, see PetaLinux KICKstart
      i. Use TE Template from /os/petalinux

7. Add Linux files (uboot.elf and image.ub) to prebuilt folder
   a. "prebuilt\os\petalinux\<ddr size>" or "prebuilt\os\petalinux\<short name>"
      Notes: Scripts select "prebuilt\os\petalinux\<short name>", if exist, otherwise
           "prebuilt\os\petalinux\<DDR size>" of the selected device

8. Generate Programming Files with HSI/SDK
   a. Run on Vivado TCL: TE::sw_run_hsi
      Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
   b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk
      Note: See SDK Projects

14 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart
15 https://wiki.trenz-electronic.de/display/PD/SDK+Projects
6 Launch

6.1 Programming

⚠️ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging](http://www.trenz-electronic.de)

6.1.1 QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp u-boot
   Note: To program with SDK/Vivado GUI, use special FSBL (zynq_fsbl_flash) on setup
   optional "TE::pr_program_flash_binfile -swapp hello_te0720" possible
4. Copy image.ub on SD-Card
5. Insert SD-Card

6.1.2 SD

1. Copy image.ub and Boot.bin on SD-Card.
   • For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Set Boot Mode to SD-Boot.
   • Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

6.1.3 JTAG

Not used on this Example.

6.2 Usage

1. Prepare HW like described on section Programming (see page 16)
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)
   Note: See TRM of the Carrier, which is used.
4. Power On PCB
   Note: 1. Zynq Boot ROM loads FSBL from SD into OCM, 2. FSBL loads U-boot from SD into DDR, 3. U-boot load Linux from SD into DDR

---

6.2.1 Linux

1. Open Serial Console (e.g. putty)
   a. Speed: 115200
   b. COM Port: Win OS, see device manager, Linux OS see `dmesg | grep tty` (UART is *USB1)

2. Linux Console:
   Note: Wait until Linux boot finished For Linux Login use:
   a. User Name: root
   b. Password: root

3. You can use Linux shell now.
   a. I2C 0 Bus type: `i2cdetect -y -r 0`
   b. I2C 1 Bus type: `i2cdetect -y -r 1`
   c. RTC check: `dmesg | grep rtc`
   d. ETH0 works with `udhcpc`
   e. USB: insert USB device

4. Option Features
   a. Webserver to get access to Zynq
      i. insert IP on web browser to start web interface
   b. init.sh scripts
      i. add init.sh script on SD, content will be load automatically on startup (template included in `./misc/SD`)

6.2.2 Vivado HW Manager

Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder

- Monitoring: PHY LED

![Vivado Hardware Manager](image)
7 System Design - Vivado

7.1 Block Design

Figure 2: Block Design

7.1.1 PS Interfaces

<table>
<thead>
<tr>
<th>Type</th>
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<tr>
<td>DDR</td>
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<td>UART1</td>
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<tr>
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<tr>
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<td>MIO</td>
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<td>EMIO</td>
</tr>
<tr>
<td>WDT</td>
<td>EMIO</td>
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</table>

## 7.2 Constrains

### 7.2.1 Basic module constrains

```bash
# _i_bitgen_common.xdc

set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
```

```bash
# _i_common.xdc

set_property BITSTREAM.CONFIG.UNUSEDPIN PULLUP [current_design]
```
7.2.2 Design specific constrain

_zip_TE0720-SC.xdc

# Constraints for System controller support logic
#
set_property PACKAGE_PIN K16 [get_ports PL_pin_K16]
set_property PACKAGE_PIN K19 [get_ports PL_pin_K19]
set_property PACKAGE_PIN K20 [get_ports PL_pin_K20]
set_property PACKAGE_PIN L16 [get_ports PL_pin_L16]
set_property PACKAGE_PIN M15 [get_ports PL_pin_M15]
set_property PACKAGE_PIN N15 [get_ports PL_pin_N15]
set_property PACKAGE_PIN N22 [get_ports PL_pin_N22]
set_property PACKAGE_PIN P16 [get_ports PL_pin_P16]
set_property PACKAGE_PIN P22 [get_ports PL_pin_P22]

# If Bank 34 is not 3.3V Powered need change the IOSTANDARD
#
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_P22]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_P16]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_N22]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_N15]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_M15]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_L16]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_K20]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_K19]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_K16]
8 Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects

8.1 Application

Template location: ./sw_lib/sw_apps/

8.1.1 zynq_fsbl

TE modified 2018.3 FSBL

General:

- Modified Files: main.c, fsbl_hooks.h/.c (search for 'TE Mod' on source code)
- Add Files: te_fsbl_hooks.h/.c (for hooks and board)
- General Changes:
  - Display FSBL Banner and Device ID

Module Specific:

- Add Files: all TE Files start with te_*
  - READ MAC from EEPROM and make Address accessible by UBOOT (need copy defines on uboot platform-top.h)
  - CPLD access
  - Read CPLD Firmware and SoC Type
  - Configure Marvell PHY
  - USB PHY Reset
  - Configure LED usage

8.1.2 zynq_fsbl_flash

TE modified 2018.3 FSBL

General:

- Modified Files: main.c
- General Changes:
  - Display FSBL Banner
  - Set FSBL Boot Mode to JTAG
  - Disable Memory initialisation

8.1.3 hello_te0720

Hello World App in Endless loop.

17 https://wiki.trenz-electronic.de/display/PD/SDK+Projects
8.1.4 u-boot

U-Boot.elf is generated with PetaLinux. SDK/HSi is used to generate Boot.bin.
9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux Kickstart

9.1 Config

Start with petalinux-config or petalinux-config --get-hw-description

Changes:

- CONFIG_SUBSYSTEM_SERIAL_PS7_UART_0_SELECT=y
- CONFIG_SUBSYSTEM_SERIAL_IP_NAME="ps7_uart_0"
- CONFIG_SUBSYSTEM_NETBOOT_OFFSET=0x8000000 ! Must be done manually for 256MB DDR only → not done on with HDF import from the template!

9.2 U-Boot

Start with petalinux-config -c u-boot

Changes:

- CONFIG_ENV_IS_NOWHERE=y
- # CONFIG_ENV_IS_IN_SPI_FLASH is not set

Change platform-top.h:

18 https://wiki.trenz-electronic.de/display/PD/PetaLinux+Kickstart
#include <configs/platform-auto.h>
#define CONFIG_SYS_BOOTM_LEN 0xF000000
#define DFU_ALT_INFO_RAM "
  "dfu_ram_info=" 
  "setenv dfu_alt_info " 
  "image.ub ram $netstart 0x1e00000\0" 
  "dfu_ram=run dfu_ram_info && dfu 0 ram 0\0" 
  "thor_ram=run dfu_ram_info && thordown 0 ram 0\0"

#define DFU_ALT_INFO_MMC "
  "dfu_mmc_info=" 
  "set dfu_alt_info " 
  "${kernel_image} fat 0 1\\;" 
  "dfu_mmc=run dfu_mmc_info && dfu 0 mmc 0\0" 
  "thor_mmc=run dfu_mmc_info && thordown 0 mmc 0\0"

/*Required for uartless designs */
#ifndef CONFIG_BAUDRATE
#define CONFIG_BAUDRATE 115200
#endif
#undef CONFIG_DEBUG_UART
#endif

/*Define CONFIG_ZYNQ_EEPROM here and its necessaries in u-boot menuconfig if you had EEPROM memory. */
#ifndef CONFIG_ZYNQ_EEPROM
#define CONFIG_SYS_I2C_EEPROM_ADDR_LEN 1
#define CONFIG_SYS_I2C_EEPROM_ADDR 0x54
#define CONFIG_SYS_EEPROM_PAGE_WRITE_BITS 4
#define CONFIG_SYS_EEPROM_PAGE_WRITE_DELAY_MS 5
#define CONFIG_SYS_EEPROM_SIZE 1024 /* Bytes */
#define CONFIG_SYS_I2C_MUX_ADDR 0x74
#define CONFIG_SYS_I2C_MUX_EEPROM_SEL 0x4
#endif

#define CONFIG_PREBOOT "echo U-BOOT for petalinux;echo importing env from FSBL 
shared area at 0xFFFFFC00; if test *0xFFFFFC00 == 0xCAFEBABE; then echo Found valid 
magic; env import -t 0xFFFFFC04; fi;setenv preboot; echo; dhcp"
9.3 Device Tree

```
#include/ "system-conf.dtsi"
{

/* default */

/* QSPI PHY */
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    }
};

/* ETH PHY */
&gem0 {
    phy-handle = <&phy0>;
    mdio {
        #address-cells = <1>;
        #size-cells = <0>;
        phy0: phy@0 {
            compatible = "marvell,88e1510";
            device_type = "ethernet-phy";
            reg = <0>;
        }
    }
};

/* USB PHY */

{
    usb_phy0: usb_phy@0 {
        compatible = "ulpi-phy";
        //compatible = "usb-nop-xceiv";
        #phy-cells = <0>;
        reg = <0xe0002000 0x1000>;
        view-port = <0x0170>;
        drv-vbus;
    }
};

&usb0 {
    dr_mode = "host";
    //dr_mode = "peripheral";
```
usb-phy = &usb_phy0;
};

/* I2C need I2C1 connected to te0720 system controller ip */
&i2c1 {
    iexp@20 { // GPIO in CPLD
        #gpio-cells = <2>;
        compatible = "ti,pcf8574";
        reg = <0x20>;
        gpio-controller;
    };
    iexp@21 { // GPIO in CPLD
        # gpio-cells = <2>;
        compatible = "ti,pcf8574";
        reg = <0x21>;
        gpio-controller;
    };
    rtc@6F { // Real Time Clock
        compatible = "isl12022";
        reg = <0x6F>;
    };
};

9.4 Kernel

Start with petalinux-config -c kernel
Changes:
- CONFIG_RTC_DRV_ISL12022=y

9.5 Rootfs

Start with petalinux-config -c rootfs
Changes:
- CONFIG_i2c-tools=y
- CONFIG_busybox-httpd=y (for web server app)

9.6 Applications

9.6.1 startup

Script App to load init.sh from SD Card if available.
See: \os\petalinux\project-spec\meta-user\recipes-apps\startup\files
9.6.2 webfwu

Webserver application assemble for Zynq access. Need busybox-httpd
10 Additional Software

No additional software is needed.
# 11 Appx. A: Change History and Legal Notices

## 11.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

<table>
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<th>Authors</th>
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<td>John Hartfiel&lt;br&gt;20</td>
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<td>v.33</td>
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20 [https://wiki.trenz-electronic.de/display/~j.hartfiel](https://wiki.trenz-electronic.de/display/~j.hartfiel)
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\(^{24}\)http://guidance.echa.europa.eu/
\(^{25}\)https://echa.europa.eu/candidate-list-table
\(^{26}\)http://www.echa.europa.eu/

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