MIO[29..26] -> PJTAG1

VCC064, VCC065, VCC066 ->> max. 1.8V (HP bank's)
CHANGES REV01 to REV02

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1) Added MAC EEPROM (slave address)
2) LIB components update
3) Fixed SD Card connection
4) Fixed sense connection from DCDC
5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
6) Added resistors for variants (ZU+ with/without VCU)
7) Added termination resistors (240R) to VRP pins for all HP-banks