Title: TE0820 - DDR4_2_RAM

Date: 2018-03-28
Number: 03CG-1IA
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CHANGES REV01 to REV02

- Added MAC EEPROM (slave address)
- LIB components update
- Fixed SD Card connection
- Fixed sense connection from DCDC
- Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
- Added resistors for variants (ZU+ with/without VCU)
- Added termination resistors (240R) to VRP pins fro all HP-banks

CHANGES REV02 to REV03

- Fixed VCU connection: add additional DCDC (0.9V)
- LIB components update
- Change package 1K resistors (0402 -> 0201)
- Added LEDs (1x user LED, 1x LED for ERR_STATUS, 1xLED for ERR_OUT)
- Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit)
- Added additional DCDCs (PL_VCCINT_IO, PS_FP0V85)
- Changed DCDC (U5) 6A (optional 4A)