<table>
<thead>
<tr>
<th>Layer</th>
<th>Component</th>
<th>Description</th>
</tr>
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<tr>
<td>B25_L1_P</td>
<td>B25_L1_N</td>
<td>Component description</td>
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<tr>
<td>B44_L1_P</td>
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<td>B26_L1_P</td>
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<tr>
<td>B26_L2_P</td>
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<tr>
<td>B26_L3_P</td>
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<td>B26_L6_P</td>
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**Title:** TE0820 - HD Banks

**Date:** 2018-03-28

**Rev.:** 03

**Filename:** B_HD.SchDoc
Title: PS_DDR

A4 Number: TE0820_03EG-1EA

Date: 2018-03-28

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File name: PS_DDR.SchDoc
Title: TE0820 - POWER_1

Number: TE0820 03EG-1EA

Rev. 03

Date: 2018-03-29

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Filename: POWER_1.SchDoc

Diagram showing circuit diagrams of TPS82085SIL and other components.
CHANGES REV01 to REV02

1) Added MAC EEPROM (slave address)
2) LIB components update
3) Fixed SD Card connection
4) Fixed sense connection from DCDC
5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
6) Added resistors for variants (ZU+ with/without VCU)
7) Added termination resistors (240R) to VRP pins for all HP-banks

CHANGES REV02 to REV03

1) Fixed VCU connection: add additional DCDC (0.9V)
2) LIB components update
3) Change package 1K resistors (0402 -> 0201)
4) Added LEDs (1x user LED, 1x LED for ERR_STATUS, 1xLED for ERR_OUT)
5) Change obsolete 2SPI Flash (256MBit) -> 2SPI Flash (512MBit)
6) Added additional DCDCs (PL_VCCINT_IO, PS_FP0V85)
7) Changed DCDC (U5) 6A (optional 4A)