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Title:
TE0820 - B2B Connectors

PLL CLK IN
PS_GTR CLK IN

B65(HP) 16 IO, 8 LVDS Pairs
USB OTG
ETH SGMII
PS_GTR 4 Lanes
PS_GTR CLK IN
PLL CLK IN

Vin

B65(HP) 18 IO, 9 LVDS Pairs
B64(HP) 50 IO, 24 LVDS Pairs

VCCO64, VCCO65, VCCO66 --- max. 1.8V (HP bank’s)

MIO[29..26] -> PTAG1
CHANGES REV01 to REV02

1) Added MAC EEPROM (slave address)
2) LIB components update
3) Fixed SD Card connection
4) Fixed sense connection from DCDC
5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
6) Added resistors for variants (ZU+ with/without VCU)
7) Added termination resistors (240R) to VRP pins for all HP-banks

CHANGES REV02 to REV03

1) Fixed VCU connection: add additional DCDC (0.9V)
2) LIB components update
3) Change package 1K resistors (0402 -> 0201)
4) Added LEDs (1x user LED, 1x LED for ERR_STATUS, 1xLED for ERR_OUT)
5) Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit)
6) Added additional DCDCs (PL_VCCINT_IO, PS_FP0V85)
7) Changed DCDC (U5) 6A (optional 4A)