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### BANK 26 HD (2U4/S BANK 46 HD)

- IO_L1P_AD11P_26
- IO_L2P_AD12P_26

### BANK 44 HD (2U4/S BANK 43 HD)

- IO_L1P_AD11P_44
- IO_L2P_AD12P_44

### BANK 25 HD (2U4/S BANK 45 HD)

- IO_L1P_AD15P_25
- IO_L2P_AD16P_25

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**Title:** TE0820 - HD Banks

**Number:** TE0820 3BE21FL

**Date:** 2018-03-28

**Copyright:** Trenz Electronic GmbH / TT

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**Filename:** B_HD.SchDoc
CHANGES REV01 to REV02

1) Added MAC EEPROM (slave address)
2) LIB components update
3) Fixed SD Card connection
4) Fixed sense connection from DCDC
5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
6) Added resistors for variants (ZU+ with/without VCU)
7) Added termination resistors (240R) to VRP pins for all HP-banks

CHANGES REV02 to REV03

1) Fixed VCU connection: add additional DCDC (0.9V)
2) LIB components update
3) Change package 1K resistors (0402 -> 0201)
4) Added LEDs (1x user LED, 1x LED for ERR_STATUS, 1xLED for ERR_OUT)
5) Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit)
6) Added additional DCDCs (PL_VCCINT_IO, PS_FP0V85)
7) Changed DCDC (U5) 6A (optional 4A)