TE0820 Test Board
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<td>Technology Licenses</td>
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<td>Environmental Protection</td>
<td>23</td>
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<tr>
<td>REACH, RoHS and WEEE</td>
<td>24</td>
</tr>
</tbody>
</table>
Online version of this manual and other related documents can be found at https://wiki.trenz-electronic.de/display/PD/Trenz+Electronic+Documentation
## Overview

ZynqMP PS Design with Linux Example and simple frequency counter to measure SI5338 Reference CLK with Vivado HW-Manager.

## Key Features

- PetaLinux
- SD
- ETH
- USB
- I2C
- RTC
- FMeter
- Modified FSBL for SI5338 programming
- Special FSBL for QSPI programming

## Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Vivado</th>
<th>Project Built</th>
<th>Authors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018-06-19</td>
<td>2017.4</td>
<td>TE0820-test_board-vivado_2017.4-build_10_20180619160713.zip&lt;br&gt;TE0820-test_board_noprebuild-vivado_2017.4-build_10_20180619160728.zip</td>
<td>John Hartfiel</td>
<td>• bugfix board part files BANK1 MIO voltages&lt;br&gt;• Add &quot;dummy&quot; PS USB3 parameter so solve problems with some USB2 devices</td>
</tr>
<tr>
<td>2018-05-24</td>
<td>2017.4</td>
<td>TE0820-test_board-vivado_2017.4-build_10_20180524151356.zip&lt;br&gt;TE0820-test_board_noprebuild-vivado_2017.4-build_10_20180524151342.zip</td>
<td>John Hartfiel</td>
<td>• solved Linux Flash issue&lt;br&gt;• new assembly variant</td>
</tr>
<tr>
<td>2018-04-25</td>
<td>2017.4</td>
<td>TE0820-test_board-vivado_2017.4-build_07_20180425134435.zip&lt;br&gt;TE0820-test_board_noprebuild-vivado_2017.4-build_07_20180425134459.zip</td>
<td>John Hartfiel</td>
<td>• new assembly variants</td>
</tr>
<tr>
<td>2018-02-06</td>
<td>2017.4</td>
<td>TE0820-test_board-vivado_2017.4-build_06_20180206203359.zip&lt;br&gt;TE0820-test_board_noprebuild-vivado_2017.4-build_06_20180206203414.zip</td>
<td>John Hartfiel</td>
<td>• solved JTAG/Linux issue</td>
</tr>
<tr>
<td>2018-02-01</td>
<td>2017.4</td>
<td>TE0820-test_board-vivado_2017.4-build_05_20180201094319.zip&lt;br&gt;TE0820-test_board_noprebuild-vivado_2017.4-build_05_20180201094724.zip</td>
<td>John Hartfiel</td>
<td>• board part csv update</td>
</tr>
<tr>
<td>2018-01-24</td>
<td>2017.4</td>
<td>TE0820-test_board-vivado_2017.4-build_05_20180124085247.zip&lt;br&gt;TE0820-test_board_noprebuild-vivado_2017.4-build_05_20180124085303.zip</td>
<td>John Hartfiel</td>
<td>• rework board part files&lt;br&gt;• solved USB, QSPI and PHy issue</td>
</tr>
</tbody>
</table>
## Release Notes and Know Issues

<table>
<thead>
<tr>
<th>Issues</th>
<th>Description</th>
<th>Workaround</th>
<th>To be fixed version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash access on Linux</td>
<td>Device tree is not correct on Linux</td>
<td>add compatibility to &quot;compatible &quot;jedec, spi-nor&quot;**</td>
<td>Solved with 20180524 update</td>
</tr>
</tbody>
</table>
| USB UART Terminal is blocked / SDK Debugging is blocked | This happens only with 2017.4 Linux , when JTAG connection is established on Vivado HW Manager. | Do not use HW Manager connection, or if debugging is nessecary:  
   1. Boot linux with usb terminal  
   2. From the terminal: root root mount ifconfig eth0  
   3. Open two new SSH terminals via ethernet: root root , run user application ...  
   4. Exit and close the usb terminal | Solved with 20180206 update |

## Requirements

### Software

<table>
<thead>
<tr>
<th>Software</th>
<th>Version</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vivado</td>
<td>2017.4</td>
<td>needed</td>
</tr>
<tr>
<td>SDK</td>
<td>2017.4</td>
<td>needed</td>
</tr>
<tr>
<td>PetaLinux</td>
<td>2017.4</td>
<td>needed</td>
</tr>
<tr>
<td>SI5338 Clock Builder</td>
<td>---</td>
<td>optional</td>
</tr>
</tbody>
</table>

### Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on <design name>/board_files/*_board_files.csv
## Design supports following modules:

<table>
<thead>
<tr>
<th>Module Model</th>
<th>Board Part Short Name</th>
<th>PCB Revision Support</th>
<th>DDR</th>
<th>QSPI Flash</th>
<th>Others</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0820-ES1</td>
<td>es1</td>
<td>REV01</td>
<td>1GB</td>
<td>64</td>
<td></td>
<td>• use slower DDR speed</td>
</tr>
<tr>
<td>TE0820-02-2EG-1E</td>
<td>2eg_1e</td>
<td>REV02</td>
<td>1GB</td>
<td>64</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0820-02-2EG-1E3</td>
<td>2eg_1e</td>
<td>REV02</td>
<td>1GB</td>
<td>64</td>
<td></td>
<td>2.5 mm Samtec connectors</td>
</tr>
<tr>
<td>TE0820-02-2EG-1EA</td>
<td>2eg_1e</td>
<td>REV02</td>
<td>1GB</td>
<td>128</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0820-02-2EG-1EE</td>
<td>2eg_1ee</td>
<td>REV02</td>
<td>2GB</td>
<td>128</td>
<td></td>
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<tr>
<td>TE0820-02-2EG-1EL</td>
<td>2eg_1e</td>
<td>REV02</td>
<td>1GB</td>
<td>128</td>
<td>2.5 mm Samtec connectors</td>
<td></td>
</tr>
<tr>
<td>TE0820-02-2CG-1E</td>
<td>2cg_1e</td>
<td>REV02</td>
<td>1GB</td>
<td>64</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0820-02-2CG-1EA</td>
<td>2cg_1e</td>
<td>REV02</td>
<td>1GB</td>
<td>128</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0820-02-3EG-1E</td>
<td>3eg_1e</td>
<td>REV02</td>
<td>1GB</td>
<td>64</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0820-02-3EG-1E3</td>
<td>3eg_1e</td>
<td>REV02</td>
<td>1GB</td>
<td>64</td>
<td>2.5 mm Samtec connectors</td>
<td></td>
</tr>
<tr>
<td>TE0820-02-3EG-1EA</td>
<td>3eg_1e</td>
<td>REV02</td>
<td>1GB</td>
<td>128</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0820-02-3EG-1EL</td>
<td>3eg_1e</td>
<td>REV02</td>
<td>1GB</td>
<td>128</td>
<td>2.5 mm Samtec connectors</td>
<td></td>
</tr>
<tr>
<td>TE0820-02-3CG-1E</td>
<td>3cg_1e</td>
<td>REV02</td>
<td>1GB</td>
<td>64</td>
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<tr>
<td>TE0820-02-3CG-1EA</td>
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<td>REV02</td>
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<tr>
<td>TE0820-02-4CG-1EA</td>
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<td>REV02</td>
<td>1GB</td>
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<tr>
<td>TE0820-03-4EV-1EA</td>
<td>4ev_1e</td>
<td>REV03</td>
<td>1GB</td>
<td>128</td>
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</table>

## Design supports following carriers:

<table>
<thead>
<tr>
<th>Carrier Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0701</td>
<td>• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers</td>
</tr>
</tbody>
</table>
| TE0703        | • Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 cm carriers  
                          • Used as reference carrier. |
| TE0705        | • Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers |
## Carrier Model | Notes
--- | ---
TE0706 | Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers

| Carrier Model | Notes |
--- | ---
TEBA0841 | Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers
| No SD Slot available, pins goes to Pin Header
| For TEBA0841 REV01, please contact TE support |

### Additional HW Requirements:

| Additional Hardware | Notes |
--- | ---
USB Cable for JTAG/UART | Check Carrier Board and Programmer for correct typ |
XMOD Programmer | Carrier Board dependent, only if carrier has no own FTDI |
Cooler | It's recommended to use cooler on ZynqMP device |

### Content

For general structure and of the reference design, see Project Delivery

### Design Sources

| Type       | Location                  | Notes |
--- | --- | ---
Vivado     | <design name>/block_design<br><design name>/constraints<br><design name>/ip_lib | Vivado Project will be generated by TE Scripts |
SDK/HSI    | <design name>/sw_lib       | Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI |
PetaLinux  | <design name>/os/petalmx   | PetaLinux template with current configuration |

### Additional Sources

| Type  | Location                  | Notes |
--- | --- | ---
Si5338 | <design name>/misc/Si5338 | Si5338 Project with current PLL Configuration |

### Prebuilt

| File                      | File-Extension | Description |
--- | --- | --- |
BIF-File                  | *.bif          | File with description to generate Bin-File |
BIN-File                  | *.bin          | Flash Configuration File with Boot-Image (Zynq-FPGAs) |
BIT-File                  | *.bit          | FPGA (PL Part) Configuration File |
DebugProbes-File          | *.ltx          | Definition File for Vivado/Vivado Labtools Debugging Interface |
Diverse Reports           | ---            | Report files in different formats |
Hardware-Platform-Specification-Files | *.hdf | Exported Vivado Hardware Specification for SDK/HSI and PetaLinux |
Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0820 "Test Board" Reference Design
Design Flow

Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- Vivado/SDK/SDSoC#XilinxSoftware-BasicUserGuides
- Vivado Projects
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with ".\_create\_win\_setup.cmd" on Windows OS and "\_create\_linux\_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. \_create\_win\_setup.cmd/\_create\_linux\_setup.sh and follow instructions on shell:

2. Press 0 and enter for minimum setup

3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)

4. Create Project
   a. Select correct device and Xilinx install path on "design\_basic\_settings.cmd" and create Vivado project with "vivado\_create\_project\_guimode.cmd"
   Note: Select correct one, see TE Board Part Files
5. Create HDF and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
      Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder

6. Create Linux (bl31.elf, uboot.elf and image.ub) with exported HDF
   a. HDF is exported to "\prebuilt\hardware\<short name>"
      Note: HW Export from Vivado GUI create another path as default workspace.
   b. Create Linux images on VM, see PetaLinux KICKstart
      i. Use TE Template from /os/petalinux
         Note: run init_config.sh before you start petalinux config. This will set correct temporary path variable.

7. Add Linux files (bl31.elf, uboot.elf and image.ub) to prebuilt folder
   a. "\prebuilt\os\petalinux\default" or "\prebuilt\os\petalinux\<short name>"
      Notes: Scripts select "\prebuilt\os\petalinux\<short name>", if exist, otherwise "\prebuilt\os\petalinux\default"

8. Generate Programming Files with HSI/SDK
   a. Run on Vivado TCL: TE::sw_run_hsi
      Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
   b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk
      Note: See SDK Projects
Launch

Programming

⚠️ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging](http://www.trenz-electronic.de)

Note: Depending on CPLD Firmware and Boot Mode settings, QSPI boot with Linux image on SD or complete SD Boot is possible.

QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_gui_mode.cmd" or if not created, create with "vivado_create_project_gui_mode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp u-boot
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup
4. Copy image.ub on SD-Card
   • For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
5. Insert SD-Card

SD

Use this description for CPLD Firmware with SD Boot selectable.

1. Copy image.ub and Boot.bin on SD-Card.
   • For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Insert SD-Card in SD-Slot.

JTAG

Not used on this Example.

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card or QSPI as Boot Mode (Depends on used programming variant)
   Note: See TRM of the Carrier, which is used.
4. Power On PCB
   Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from SD/QSPI Flash into OCM, 2. FSBL loads ATF(bl31.elf) and U-boot from SD into DDR, 3. U-boot load Linux from SD into DDR

Linux

1. Open Serial Console (e.g. putty)
   a. Speed: 115200
   b. COM Port: Win OS, see device manager, Linux OS see dmesg grep tty (UART is *USB1)

2. Linux Console:
   Note: Wait until Linux boot finished For Linux Login use:
   a. User Name: root
   b. Password: root

3. You can use Linux shell now.
   a. I2C 0 Bus type: i2cdetect -y -r 0
   b. RTC check: dmesg grep rtc
   c. ETH0 works with udhcpc
   d. USB type "lsusb" or connect USB2.0 device

Vivado HW Manager

SI5338_CLK0 Counter:

1. Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).
   a. Set radix from VIO signals to unsigned integer.
      Note: Frequency Counter is inaccurate and displayed unit is Hz

SI5338 CLK is configured to 200MHz by default.

PHY LEDS

- See: TE0820-REV01_REV02 CPLD#X0/X1Pin

CPLD Firmware:

- See: TE0820-REV01_REV02 CPLD#X0/X1Pin
**System Design - Vivado**

**Block Design**

Activated interfaces:

<table>
<thead>
<tr>
<th>Type</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR</td>
<td></td>
</tr>
<tr>
<td>QSPI</td>
<td>MIO</td>
</tr>
<tr>
<td>SD0</td>
<td>MIO</td>
</tr>
<tr>
<td>SD1</td>
<td>MIO</td>
</tr>
<tr>
<td>I2C0</td>
<td>MIO</td>
</tr>
<tr>
<td>UART0</td>
<td>MIO</td>
</tr>
</tbody>
</table>
Type | Note
---|---
GPIO0 | MIO
SWDT0..1 | MIO
TTC0..3 | MIO
GEM3 | MIO
USB0 | MIO

## Constrains

### Basic module constrains

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

### Design specific constrain

```
set_property PACKAGE_PIN K9 [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property IOSTANDARD LVDS [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property DIFF_TERM TRUE [get_ports {SI5338_CLK0_D_clk_p[0]}]

set_property PACKAGE_PIN H1 [get_ports {x0_firmware[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x0_firmware[0]}]
set_property PACKAGE_PIN J1 [get_ports {x1_phy_led[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x1_phy_led[0]}]
```
Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects

Application

zynqmp_fsbl

TE modified 2017.4 FSBL

Changes:

- Si5338 Configuration, ETH+OTG Reset over GPIO see xfsbl_board.c, xfsbl_board.h
- Add register_map.h, si5338.c, si5338.h

zynqmp_fsbl_flash

TE modified 2017.4 FSBL

Changes:

- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation

zynqmp_pmufw

Xilinx default PMU firmware.

Hello TE0820

Hello TE0820 is a Xilinx Hello World example as endless loop instead of one console output.

U-Boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.
Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

Config

No changes.

U-Boot

- Change platform-top.h

```c
#include <configs/platform-auto.h>
#define CONFIG_SYS_BOOTM_LEN 0xF000000

#define DFU_ALT_INFO_RAM 
   "dfu_ram_info" 
   "setenv dfu_alt_info " 
   "image.ub ram ${netstart} 0x1e000000\0" 
   "dfu_ram=run dfu_ram_info && dfu 0 ram 0\0" 
   "thor_ram=run dfu_ram_info && thordown 0 ram 0\0"

#define DFU_ALT_INFO 
   DFU_ALT_INFO_RAM

/*Required for uartless designs */
#ifndef CONFIG_BAUDRATE
#define CONFIG_BAUDRATE 115200
#endif
#endif

/*select sd instead of mmc for autoboot */

#define CONFIG_BOOTCOMMAND "run uenvboot; mmcinfo & & fatload mmc 1 ${netstart} 
   ${kernel_image}; bootm ${netstart}"`
```

Device Tree

```c
#include/ "system-conf.dtsi"
/
};

/* SDIO */
```
&sdhci1 {
    disable-wp;
    no-1-8-v;
};

/* ETH PHY */
&gem3 {
    status = "okay";
    ethernet_phy0: ethernet-phy@0 {
        compatible = "marvell,88e1510";
        device_type = "ethernet-phy";
        reg = <1>;
    };
};

/* USB 2.0 */
&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    maximum-speed = "high-speed";
    /delete-property/phy-names;
    /delete-property/phys;
    /delete-property/snps,usb3_lpm_capable;
};

/* QSPI PHY */
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0>/;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};

/* DMA not used: Reduce error messages on linux. */
&lpd_dma_chan1 {
    status = "disabled";
};
&lpd_dma_chan2 {
    status = "disabled";
};
&lpd_dma_chan3 {
    status = "disabled";
};
&lpd_dma_chan4 {
    status = "disabled";
};
&lpd_dma_chan5 {
    status = "disabled";
};
&lpd_dma_chan6 {
### Kernel

Deactivate:

- `CONFIG_CPU_IDLE` (only needed to fix JTAG Debug issue)
- `CONFIG_CPU_FREQ` (only needed to fix JTAG Debug issue)

### Rootfs

Activate:

- `i2c-tools`

### Applications

**startup**

Script App to load init.sh from SD Card if available.

See: `/os/petalinux/project-spec/meta-user/recipes-apps/startup/files`
Additional Software

SI5338

Download ClockBuilder Desktop for SI5338

1. Install and start ClockBuilder
2. Select SI5338
3. Options Open register map file
   Note: File location <design name>/misc/Si5338/RegisterMap.txt
4. Modify settings
5. Options save C code header files
6. Replace Header files from FSBL template with generated file
### Appx. A: Change History and Legal Notices

#### Document Change History

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2018-09-18