tílt: TE0841
num: TE0841
41C21-A
rev: 02
date: 2018-03-14
copyright: Trenz Electronic GmbH / TT
filename: FPGA-B68.SchDoc
CHANGES REV01 TO REV01A (08.16.2017):

1) U1: changed schematic symbol. Next pins swapped to match same polarity order:
   -- AE13 (IO_L6P_T0U_N10_AD6P_64)/AE12 (IO_L6N_T0U_N11_AD6N_64)
   -- J5 (IO_L18P_T2U_N10_AD2P_66)/J4 (IO_L18N_T2U_N11_AD2N_66)

2) Net names changed (no electrical changes):
   JM1: swapped signals B64_L6:
   -- B64_L6_N - pin 40 (was pin 42)
   -- B64_L6_P - pin 42 (was pin 40)
   JM3: swapped signals B64_L6:
   -- B66_L18_N - pin 52 (was pin 54)
   -- B66_L18_P - pin 54 (was pin 52)

CHANGES REV01A TO REV02 (03.2018):

2) Fixed sense connection on DCDC
3) U6: changed SPI flash chip: N25Q256AI1E1240E -> N25Q512A11G1240E
4) Full update LIB
5) Added additional resistors for support 16GBit DDR chips
6) Added strong pull-down to EN_PLL
7) Added additional testpoints for I2C bus
8) Added additional MEMS oscillator (25MHz)
9) Changed pull-up power supply VIN -> 3.3VIN on the PG_DDR net
10) Added pull-down on the EN_DDR