REV02

----------------------------------
1) changed VCCIO (3.3V -> VIN33) on XMOD
2) added pull-up resistors R22, R24 to JTAGSEL, BOOT_MODE1, BOOT_MODE2
3) changed micro-USB
4) changed magjack connectors
5) lib component update
6) added thermal vias to mounting holes
7) added visual serial number
8) changed 2.1mm power jack THT on SMD

REV03

----------------------------------
1) 1) New design of reset circuit, JB2 pin 89 and F9 B30 was connected by net RST_STATUS (Source - CPLD TE0729). JB2 pin 91, JB3 pin 11 (XMOD), S1 (button) connected by net NRST_IN (connected to CPLD TE0729 and supervisor U21 pin 3 (manual reset)
2) ETH1_CTREF, ETH2_CTREF disconnected from JB2. C3/C4 and C5/C6 disconnected from one another.
3) J3 pin 10, J4 pin 8, J5 pin 8 connected to net FGND.