Title: TEB0745

A4 Number: TEB0745

Rev. 02

Date: 2016-10-11

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Filename: J2.schdoc
The module signal ground contacts, VeER and VeET, should be isolated from the module case.
REV02:
1) U16 I2C expander: address set to 0x72
2) U33 EEPROM: address set to 0x51. Added variant to set address 0x52.
3) Changed power up sequence: 24V_FUSED -> 3.3V (Module power up) -> 5V -> VCCIO18, VCC_HR_B, 3.3V_SFP
4) Fixed PCB patch: U6 pin 18 connected to 5V, pin 19 connected to GND.
5) JTAG connector J30 VREF (pin 2) and XMOD VIO (pin 6) connected to 3.3V. XMOD IO A, B, E, G connected to module MIO via level translator U8.
6) Pull-ups for BOOTMODE and PS_SW (DIP switch S1), RST_IN_N and USR_BTN (front panel buttons S2, S3) changed from VCCIO18 to PS_1.8V. JTAG EN connected to 3.3V via DIP switch (S1).
7) Added switch S4 for selecting of output voltage of DCDC U7 (VCC_HR_B, HR banks VCCO)

REV02a (06.12.2018):
1) Resistors R14 and R15 was replaced by 953R (was 5K1)
2) Resistor R5 was replaced by 5K1, R8 by 953R (was 9K09 and 1K69 respectively)