Remove for programming OTP ROM

Test point 1mm
**LAYOUT NOTES:**
Each member of a High-Speed differential pair should be no more than 1.25 mm.
Each member of a SuperSpeed differential pair should be no more than 0.13 mm.

**RESETN pin should be held LOW until both supplies become stable.**

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**EEPROM: 0x51 (0b1010001x)**

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**Date:** 2016-08-29

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REV03
1) Added 2.5V option for clock source U45
2) Net B64_T0 terminated via 240 Ohm resistor to GND.
3) Nets B64_T1..T3 connected to CPLD
4) Nets SFPw_LOS and SFPw_TX_DIS connected to CPLD (# = 1..2)
5) Added 4-pin connector for FAN2 (12V). Added high side switch like option for FAN without control signals.
6) Added net SC_J08 between CPLD1 and CPLD2 (Bank 3V3_SB)
7) Deleted USB3.0 port (J18)
8) Port USB2.0 replaced to USB3.0 (J8, front panel)
9) Replaced USB HUB USB5537B to CYUSB3324 (U4)