Distance Holder M3x5 Male/Female

GND

PAD1

PAD2

PAD3

PAD4

TE_76x52mm_3N_Snap

Washer M3

Serrated Washer M3

Nut M3

Washer M3

Serrated Washer M3

Nut M3
LAYOUT NOTES:
Each member of a High-Speed differential pair should be no more than 1.25 mm.
Each member of a SuperSpeed differential pair should be no more than 0.13 mm.

RESETHN pin should be held LOW until both supplies become stable.

CLK: 0x60 (or 0x58)
Title: TEBF0808 - FMC

Number: TEBF0808

Rev. 04

Date: 2016-09-29
Copyright: Trenz Electronic GmbH

Filename: FMC PWR.SchDoc
Date: 07.05.2019
Number: TEBF0808
Title: TEBF0808 - CLK
Copyright: Trenz Electronic GmbH
Filename: CLK_MUX.schdoc
LAYOUT NOTES:
- Signal trace length skew constraints
- Mismatch within DAT0-DAT7 < 250 mil
- CLK to DAT0-DAT7 mismatch < 250 mil
- CLK to CMD mismatch < 250 mil
- CLK to RST_N mismatch < 1000 mil

Title: TEBF0808 - eMMC
Number: TEBF0808
Rev. 04
Date: 2016-09-29
Copyright: Trenz Electronic GmbH
Page 25 of 36
Filename: eMMC.SchDoc
Clock source for audio codec.
REV03
1) Added 2.5V option for clock source U45
2) Net B64_T0 terminated via 240 Ohm resistor to GND.
3) Nets B64_T1, T3 connected to CPLD
4) Nets SPIRX_LOS and SPIRX_DIS connected to CPLD (R = 1..2)
5) Added 4-pin connector for FAN2 (12V). Added high side switch like option for FAN without control signals.
6) Added net SC_JOB between CPLD1 and CPLD2 (Bank 3VS_18)
7) Deleted USB0.0 port (J18)
8) Port USB2.0 replaced to USB3.0 (J8, front panel)
9) Replaced USB Hub USB5537B to CYUSB3324 (J4)

REV04
1) P and N lanes swapped in FMC clock signal pairs B228_CLK0 and B229_CLK0
2) Added additional FAN connector (J35)
3) New control circuit for external beeper
4) Layout and routing improvements
   -- 10.08.2018
5) Resistors R130-131, R173-174 replaced from 4.99k to 2k
   -- 26.03.2019
6) VY: Resistor R65 replaced from 8.06k to 1k (assembly variant "A")
7) VY: Page 21: EEPROM I2C address correction
8) VY: Clock source U6 (100MHz) populated (assembly variant "A")