U_J1
J1.schdoc
U_J2
J2.schdoc
U_J3
J3.schdoc
U_J4
J4.schdoc

Washer M3
Serrated Washer M3
Nut M3

Distance Holder M3x5 Male/Female

SNAP1
PAD1
PAD2
PAD3
PAD4

GND
GND
GND
GND

Distancce Holder M3x5 Male/Female

Washer M3
Serrated Washer M3
Nut M3
Each member of a High-Speed differential pair should be no more than 1.25 mm.
Each member of a SuperSpeed differential pair should be no more than 0.13 mm.

RESET pin should be held LOW until both supplies become stable.

LAYOUT NOTES: Each member of a High-Speed differential pair should be no more than 1.25 mm.
Each member of a SuperSpeed differential pair should be no more than 0.13 mm.

RESTART pin should be held LOW until both supplies become stable.

LAYOUT NOTES: Each member of a High-Speed differential pair should be no more than 1.25 mm.
Each member of a SuperSpeed differential pair should be no more than 0.13 mm.

RESET pin should be held LOW until both supplies become stable.
**Title:** TEBF0808 - I2C System

**Number:** TEBF0808

**Date:** 2016-09-29

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**Page:** 21 of 36
REV03
1) Added 2.5V option for clock source U45
2) Net B64_T0 terminated via 240 Ohm resistor to GND.
3) Nets B64, TL, T3 connected to CPLD
4) Nets SFP_LOS and SFP_TX_DIS connected to CPLD (R = 1..2)
5) Added 4-pin connector for FAN2 [12V]. Added high side switch like option for FAN without control signals.
6) Added net SC_JOB between CPLD1 and CPLD2 (Bank 3V3_SB)
7) Deleted USB0.0 port [118]
8) Port USB2.0 replaced to USB3.0 [18, front panel]
9) Replaced USB HUB USB5537B to CYUSB3324 [u4]

REV04:
1) P and N lanes swapped in FMC clock signal pairs B228_CLK0 and B229_CLK0
2) Added additional FAN connector [j35]
3) New control circuit for external beeper
4) Layout and routing improvements
   – 10.08.2018:
5) Resistors R130-131, R173-174 replaced from 4.99k to 2k
   – 26.03.2019
6) VY: Resistor R65 replaced from 8.06k to 1k (assembly variant “A”)
7) VY: Page 21: EEPROM I2C address correction
8) VY: Clock source U6 [100Mhz] populated (assembly variant “A”)