CHANGES REV01 to REV02

1) MAC EEPROM Address patch fixed on PCB
2) lib components update
RESERVED for additional 8 GTX lanes
Title: TE0745 - Zynq_MIO_Banks
A4 Number: 14 91C11-A
Rev. 02
Date: 2016-04-28
Copyright: Trenz Electronic GmbH / TT
Page14 of 25
Filename: MIO_B500.SchDoc
Slave ADDR:

for RTC registers: 110111

for User SRAM: 1010111
Pre-bias assembly option

R39 R40 MODE EN63AOQI

OK X enable pre-bias start-up
X OK disable pre-bias start-up

Soft start 3ms
TE0745 - Power3

Date: 2016-04-29

Title: TE0745 - Power3

Number: 24

Filename: POWER_3.SchDoc
DCDC 1V, 12A

EN.PL

DCDC 1.8V, 3A

PG.PL

DCDC 1.45V, 3A

PL_GT_1V45

DCDC 1.25V, 3A

PG.PL

LDO 1.2V, 3A

MGTAVTT

LDO 1.0V, 3A

MGTAUX

LDO 1.8V, 0.35A

PG

VCCINT

VCCPINT

PS_3.3V

from B2B connectors

DCDC 1V, 3A

EN

PG.VCCINT

DCDC 1.8V, 3A

EN

PG.VCCINT

DCDC 1.35V, 3A

PG

PWR_PS_OK

PS_1.8V

1.8V PS

DDR3.L

(3.3V)

PL_VIN

PG_VCCINT

VCCINT

PWR.PL_OK

MGTAVCC

(3.3V)

PS_VIN

PG_VCCINT

VCCPINT

CPU Core

(3.3V)

from B2B connectors

FPGA Core

PG

VCCINT

PL_1.8V

1.8V PL

1.8V PS

(3.3V)

from B2B connectors

1.35V

DDR3.L

1.35V DDR3_L

PWR_PS_OK

PG

(3.3V)

from B2B connectors

PS_3.3V