**Title:** TE0803 - HD Banks

**Date:** 2018-05-21

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**Filename:** B_HD_SchDoc
CHANGES REV01 a (20.11.2017):

1) VCU voltage set to 0.9V, R20 changed to 40K, PL_VCU_1V0 renamed to PL_VCU_0V9.

CHANGES REV02 (20.06.2018):

1) Added LDO to DDR_PLL
2) All differential pairs with length matched within tolerance 0.1mm (excluding package delays)
3) Added MAC EEPROM U28
4) VPS_MGTRAVCC set to 0.85V
5) Added pull-up resistors R68, R69