Title: TE0803 - PS_DDR

A4 Number: TE0803 48E21-L

Date: 2019-02-21 Copyright: Trenz Electronic GmbH / T

Filename: PS_DDR.SchDoc

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Diagram showing various components and connections related to memory and power distribution in a circuit.
CHANGES REV01a (20.11.2017):
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1) VCU voltage set to 0.9V, R20 changed to 40K, PL_VCU_1V0 renamed to PL_VCU_0V9.

CHANGES REV02 (20.06.2018):
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1) Added LDO to DDR_PLL
2) All differential pairs with length matched with tolerance 0.1mm (excluding package delays)
3) Added MAC EEPROM U28
4) VPS_MGTRAVCC set to 0.85V
5) Added pull-up resistors R68,R69

CHANGES REV03 (21.02.2019):
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1) Added support of DDR DDR4
2) Added support of Low power FPGA (-L1/L2).
3) Revised testpoints.
4) Revised J1-J4 connectors net label style