Changes REV01a (20.11.2017):

1) VCU voltage set to 0.9V, R20 changed to 40K, PL_VCU_1V0 renamed to PL_VCU_0V9.

Changes REV02 (20.06.2018):

1) Added LDO to DDR_PLL
2) All differential pairs with length matched with tolerance 0.1mm (excluding package delays)
3) Added MAC EEPROM U28
4) VPS_MGTRAVCC set to 0.85V
5) Added pull-up resistors R68,R69

Changes REV03 (21.02.2019):

1) Added support of DDP DDR4
2) Added support of Low power FPGA (-L1/L2).
3) Revised testpoints
4) Revised J1-J4 connectors net label style