TE0803 - Connector J1

Title: TE0803 - Connector J1
Number: 5D124-A
Rev. 03
Date: 2019-02-21
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Filename: J1.SchDoc
Remove R86 when -1LI/2LE FPGA used

Remove R87/89 when -1LI/2LE FPGA used
Title: TE0803 - POWER_4

Date: 2019-02-21
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Filename: POWER_4.SchDoc

A4 Number: TE0803 5D124-A Rev. 03

Description of the diagram:
- The diagram shows a circuit with various components such as resistors, capacitors, and diodes.
- The components are labeled with their respective values and connections.
- The schematic includes labels for power rails, control signals, and other critical points in the circuit.
- The circuit appears to be designed for power management, possibly involving voltage regulators and current sources.
CHANGES REV01a (20.11.2017):

1) VCU voltage set to 0.9V, R20 changed to 40K, PL_VCU_1V0 renamed to PL_VCU_0V9.

CHANGES REV02 (20.06.2018):

1) Added LDO to DDR_PLL
2) All differential pairs wath length matched with tollerance 0.1mm (excluding package delays)
3) Added MAC EEROM U28
4) VPS_MGTRAVCC set to 0.85V
5) Added pull-up resistors R68,R69

CHANGES REV03 (21.02.2019):

1) Added support of DDP DDR4
2) Added support of Low power FPGA (-L1/L2).
3) Revised testpoints
4) Revised J1-J4 connectors net label style