# Table of Contents

1. Table of Contents ........................................................................................................... 2
2. Table of Figures ............................................................................................................... 4
3. Table of Tables ................................................................................................................ 5
4. Overview .......................................................................................................................... 7
   4.1 Key Features ............................................................................................................... 7
4.2 Revision History ........................................................................................................... 7
4.3 Release Notes and Know Issues .................................................................................. 10
4.4 Requirements .............................................................................................................. 11
   4.4.1 Software .............................................................................................................. 11
   4.4.2 Hardware ............................................................................................................. 11
4.5 Content .......................................................................................................................... 13
   4.5.1 Design Sources ................................................................................................. 13
   4.5.2 Additional Sources ........................................................................................... 13
4.5.3 Prebuilt ................................................................................................................... 14
4.5.4 Download .............................................................................................................. 14
5. Design Flow .................................................................................................................... 15
6. Launch ............................................................................................................................ 17
   6.1 Programming ........................................................................................................... 17
   6.1.1 QSPI ................................................................................................................... 17
   6.1.2 SD ....................................................................................................................... 17
   6.1.3 JTAG .................................................................................................................... 17
6.2 Usage ............................................................................................................................ 18
   6.2.1 Linux ................................................................................................................... 18
   6.2.2 Vivado Hardware Manager ................................................................................. 18
7. System Design - Vivado .................................................................................................. 20
   7.1 Block Design ............................................................................................................ 20
   7.1.1 PS Interfaces ....................................................................................................... 20
7.2 Constrains .................................................................................................................... 21
   7.2.1 Basic module constrains .................................................................................... 21
   7.2.2 Design specific constrain ................................................................................... 22
8. Software Design - SDK/HSI ......................................................................................... 24
   8.1 Application ............................................................................................................... 24
   8.1.1 zynqmp_fsbl ....................................................................................................... 24
   8.1.2 zynqmp_fsbl_flash ............................................................................................. 24
   8.1.3 zynqmp_pmufw ................................................................................................... 24

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http://www.trenz-electronic.de
8.1.4  hello_te0803 .................................................................................................................. 24
8.1.5  u-boot .......................................................................................................................... 24
9     Software Design - PetaLinux .......................................................................................... 25
9.1   Config ............................................................................................................................ 25
9.2   U-Boot ............................................................................................................................ 25
9.3   Device Tree ..................................................................................................................... 26
9.4   Kernel ............................................................................................................................. 29
9.5   Rootfs .............................................................................................................................. 29
9.6   Applications .................................................................................................................... 29
9.6.1 startup ......................................................................................................................... 29
10   Additional Software ......................................................................................................... 30
10.1  SI5338 ............................................................................................................................ 30
11   Appx. A: Change History and Legal Notices ................................................................... 31
11.1  Document Change History ............................................................................................ 31
11.2  Legal Notices ................................................................................................................ 32
11.3  Data privacy .................................................................................................................. 32
11.4  Document Warranty ...................................................................................................... 32
11.5  Limitation of Liability .................................................................................................... 32
11.6  Copyright Notice .......................................................................................................... 32
11.7  Technology Licenses ..................................................................................................... 32
11.8  Environmental Protection .............................................................................................. 32
11.9  REACH, RoHS and WEEE ........................................................................................... 33
2 Table of Figures
3 Table of Tables
Online version of this manual and other related documents can be found at https://wiki.trenz-electronic.de/display/PD/Trenz+Electronic+Documentation
4 Overview

Linux with basic periphery of TE0808 Starterkit (TEBF0808 Carrier).

4.1 Key Features

- TEBF0808
- Linux
- USB
- ETH
- PCIe
- SATA
- SD
- I2C
- RGPIO
- DP
- user LED access
- Modified FSBL for Si5338 programming
- Special FSBL for QSPI Programming

4.2 Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Vivado</th>
<th>Project Built</th>
<th>Authors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018-08-14</td>
<td>2018.2</td>
<td>TE0803-Starterkit-vivado_2018.2-build_02_20180814103204.zip&lt;br&gt;TE0803-Starterkit_noprebuilt-vivado_2018.2-build_02_20180814103221.zip</td>
<td>John Hartfiel</td>
<td>• new assembly variant</td>
</tr>
<tr>
<td>Date</td>
<td>Vivado</td>
<td>Project Built</td>
<td>Authors</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>--------</td>
<td>-------------------------------------------------------------------------------</td>
<td>-------------------</td>
<td>------------------------------------------------------------------</td>
</tr>
<tr>
<td>2018-07-23</td>
<td>2018.2</td>
<td>TE0803-Starterkit-vivado_2018.2-build_02_20180723204618.zip</td>
<td>John Hartfiel</td>
<td>• correction on FSBL</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0803-Starterkit_noprebuil-vivado_2018.2-build_02_20180723204638.zip</td>
<td></td>
<td></td>
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<tr>
<td>2018-07-12</td>
<td>2018.2</td>
<td>TE0803-Starterkit_noprebuil-vivado_2018.2-build_02_20180713085800.zip</td>
<td>John Hartfiel</td>
<td>• small petalinux changes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0803-Starterkit-vivado_2018.2-build_02_20180713085740.zip</td>
<td></td>
<td>• IO renaming</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• PL Design changes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• additional notes for FSBL generated with Win SDK</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• changed *.bif</td>
</tr>
<tr>
<td>2018-05-17</td>
<td>2017.4</td>
<td>TE0803-Starterkit_noprebuil-vivado_2017.4-build_09_20180517141540.zip</td>
<td>John Hartfiel</td>
<td>• new assembly variant</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0803-Starterkit-vivado_2017.4-build_09_20180517141523.zip</td>
<td></td>
<td>• solved Linux flash issue</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0803-Starterkit-vivado_2017.4-build_07_20180411082116.zip</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Date</td>
<td>Vivado</td>
<td>Project Built</td>
<td>Authors</td>
<td>Description</td>
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<tr>
<td>------------</td>
<td>--------</td>
<td>-------------------------------------------------------------------------------</td>
<td>---------------</td>
<td>----------------------------------------------------------------------------</td>
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<tr>
<td>2018-02-13</td>
<td>2017.4</td>
<td>TE0803-Starterkit_noprebuild-vivado_2017.4-build_06_20180213120642.zip</td>
<td>John Hartfiel</td>
<td>• new assembly variant</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0803-Starterkit-vivado_2017.4-build_06_20180213120615.zip</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2018-02-06</td>
<td>2017.4</td>
<td>TE0803-Starterkit_noprebuild-vivado_2017.4-build_05_20180206082527.zip</td>
<td>John Hartfiel</td>
<td>• same CLK for both VIO</td>
</tr>
<tr>
<td></td>
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<td>TE0803-Starterkit-vivado_2017.4-build_05_20180206082513.zip</td>
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<tr>
<td>2018-02-05</td>
<td>2017.4</td>
<td>TE0803-Starterkit_noprebuild-vivado_2017.4-build_05_20180205154248.zip</td>
<td>John Hartfiel</td>
<td>• new assembly variant</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0803-Starterkit-vivado_2017.4-build_05_20180205154230.zip</td>
<td></td>
<td>• solved JTAG/Linux issue</td>
</tr>
<tr>
<td>2018-01-31</td>
<td>2017.4</td>
<td>TE0803-Starterkit-vivado_2017.4-build_05_20180131124042.zip</td>
<td>John Hartfiel</td>
<td>• new assembly variant</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0803-Starterkit_noprebuild-vivado_2017.4-build_05_20180131124057.zip</td>
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<td></td>
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</table>
### 4.3 Release Notes and Known Issues

<table>
<thead>
<tr>
<th>Issues</th>
<th>Description</th>
<th>Workaround/Solution</th>
<th>To be fixed version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash access on Linux</td>
<td>Device tree is not correct on Linux</td>
<td>add compatibility to &quot;compatible &quot;jedec,spi-nor&quot;&quot;</td>
<td><strong>Solved</strong> with 20180517 update</td>
</tr>
<tr>
<td>USB UART Terminal is blocked / SDK Debugging is blocked</td>
<td>This happens only with 2017.4 Linux, when JTAG connection is established on Vivado HW Manager.</td>
<td>Do not use HW Manager connection, or if debugging is necessary: 1. Boot linux with usb terminal 2. From the terminal: root mount ifconfig eth0 3. Open two new SSH terminals via ethernet: root root, run user application ... 4. Exit and close the usb terminal</td>
<td><strong>Solved</strong> with 20180205 update</td>
</tr>
</tbody>
</table>
4.4 Requirements

4.4.1 Software

<table>
<thead>
<tr>
<th>Software</th>
<th>Version</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vivado</td>
<td>2018.2</td>
<td>needed</td>
</tr>
<tr>
<td>SDK</td>
<td>2018.2</td>
<td>needed</td>
</tr>
<tr>
<td>PetaLinux</td>
<td>2018.2</td>
<td>needed</td>
</tr>
</tbody>
</table>

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.¹ Complete List is available on <design name>/board_files/*/board_files.csv

Design supports following modules:

<table>
<thead>
<tr>
<th>Module Model</th>
<th>Board Part Short Name</th>
<th>PCB Revision Support</th>
<th>DDR</th>
<th>QSPI Flash</th>
<th>Others</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0803-ES1</td>
<td>es1_sk</td>
<td>REV01</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0803-01-02EG-1E</td>
<td>2eg_sk</td>
<td>REV01</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0803-01-02CG-1E</td>
<td>2cg_sk</td>
<td>REV01</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0803-01-03EG-1E</td>
<td>3eg_sk</td>
<td>REV01</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0803-01-03CG-1E</td>
<td>3cg_sk</td>
<td>REV01</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

¹ https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

Xilinx has stopped ES1 support with 2018.2, please use 2017.4 reference design
<table>
<thead>
<tr>
<th>Module Model</th>
<th>Board Part Short Name</th>
<th>PCB Revision Support</th>
<th>DDR</th>
<th>QSPI Flash</th>
<th>Others</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0803-01-02EG-1EA</td>
<td>2eg_sk</td>
<td>REV01</td>
<td>2GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0803-01-02CG-1EA</td>
<td>2cg_sk</td>
<td>REV01</td>
<td>2GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0803-01-03EG-1EA</td>
<td>3eg_sk</td>
<td>REV01</td>
<td>2GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0803-02-03EG-1EB</td>
<td>3egb_sk</td>
<td>REV02, REV01</td>
<td>4GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0803-01-03CG-1EA</td>
<td>3cg_sk</td>
<td>REV01</td>
<td>2GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0803-01-04CG-1EA</td>
<td>4cg_sk</td>
<td>REV01</td>
<td>2GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0803-01-04EV-1EA</td>
<td>4ev_sk</td>
<td>REV01</td>
<td>2GB</td>
<td>128MB</td>
<td></td>
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</tr>
<tr>
<td>TE0803-01-04EV-1E3</td>
<td>4evb_sk</td>
<td>REV02</td>
<td>4GB</td>
<td>128MB</td>
<td></td>
<td>1 mm connectors</td>
</tr>
<tr>
<td>TE0803-02-04EV-1EB</td>
<td>4evb_sk</td>
<td>REV02</td>
<td>4GB</td>
<td>128MB</td>
<td></td>
<td>1 mm connectors</td>
</tr>
<tr>
<td>TE0803-01-04EG-1IA</td>
<td>4eg_i_sk</td>
<td>REV02</td>
<td>8GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0803-01-04CG-1EB</td>
<td>4cg_sk</td>
<td>REV01</td>
<td>2GB</td>
<td>256MB</td>
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<tr>
<td>TE0803-01-05EV-1EA</td>
<td>5ev_sk</td>
<td>REV01</td>
<td>2GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0803-01-05EV-1IA</td>
<td>5ev_i_sk</td>
<td>REV01</td>
<td>2GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Note: Design contains also Board Part Files for TE0808 only configuration, this board part files are not used for this reference design.

Design supports following carriers:

<table>
<thead>
<tr>
<th>Carrier Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEBF0808</td>
<td>Used as reference carrier.</td>
</tr>
</tbody>
</table>

Additional HW Requirements:

<table>
<thead>
<tr>
<th>Additional Hardware</th>
<th>Notes</th>
</tr>
</thead>
</table>

4.5 Content

For general structure and of the reference design, see Project Delivery

4.5.1 Design Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vivado</td>
<td>&lt;design name&gt;/block_design</td>
<td>Vivado Project will be generated by TE Scripts</td>
</tr>
<tr>
<td></td>
<td>&lt;design name&gt;/constraints</td>
<td></td>
</tr>
<tr>
<td></td>
<td>&lt;design name&gt;/ip_lib</td>
<td></td>
</tr>
<tr>
<td>SDK/HSI</td>
<td>&lt;design name&gt;/sw_lib</td>
<td>Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI</td>
</tr>
<tr>
<td>PetaLinux</td>
<td>&lt;design name&gt;/os/petalinux</td>
<td>PetaLinux template with current configuration</td>
</tr>
</tbody>
</table>

4.5.2 Additional Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>SI5338</td>
<td>&lt;design name&gt;/misc/Si5338</td>
<td>SI5338 Project with current PLL Configuration</td>
</tr>
</tbody>
</table>

2 https://wiki.trenz-electronic.de/display/PD/Project+Delivery
4.5.3 Prebuilt

<table>
<thead>
<tr>
<th>File</th>
<th>File-Extension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIF-File</td>
<td>*.bif</td>
<td>File with description to generate Bin-File</td>
</tr>
<tr>
<td>BIN-File</td>
<td>*.bin</td>
<td>Flash Configuration File with Boot-Image (Zynq-FPGAs)</td>
</tr>
<tr>
<td>BIT-File</td>
<td>*.bit</td>
<td>FPGA (PL Part) Configuration File</td>
</tr>
<tr>
<td>DebugProbes-File</td>
<td>*.ltx</td>
<td>Definition File for Vivado/Vivado Labtools Debugging Interface</td>
</tr>
<tr>
<td>Diverse Reports</td>
<td>---</td>
<td>Report files in different formats</td>
</tr>
<tr>
<td>Hardware-Platform-</td>
<td>*.hdf</td>
<td>Exported Vivado Hardware Specification for SDK/HSI and PetaLinux</td>
</tr>
<tr>
<td>Specification-Files</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LabTools Project-File</td>
<td>*.lpr</td>
<td>Vivado Labtools Project File</td>
</tr>
<tr>
<td>OS-Image</td>
<td>*.ub</td>
<td>Image with Linux Kernel (On PetaLinux optional with Devicetree and RAM-Disk)</td>
</tr>
<tr>
<td>Software-Application-File</td>
<td>*.elf</td>
<td>Software Application for Zynq or MicroBlaze Processor Systems</td>
</tr>
</tbody>
</table>

4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0803 "StarterKit" Reference Design

3 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0803/Reference_Design/2018.2/StarterKit
5 Design Flow

Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- Vivado/SDK/SDSoC
- Vivado Projects
- Project Delivery

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project
   a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
      Note: Select correct one, see TE Board Part Files
      Important: Use Board Part Files, which ends with "*_tebf0808"
4. Create HDF and export to prebuild folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuild
      Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (bl31.elf, uboot.elf and image.ub) with exported HDF

---

5 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects
6 https://wiki.trenz-electronic.de/display/PD/Project+Delivery
7 https://wiki.trenz-electronic.de/display/PD/Project+Delivery#ProjectDelivery-Currentlylimitationsoffunctionality
8 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files
a. HDF is exported to "prebuilt\hardware\<short name>"
   Note: HW Export from Vivado GUI create another path as default workspace.

Create Linux images on VM, see PetaLinux KICKstart\(^9\)
   i. Use TE Template from /os/petalinux
      Note: run init_config.sh before you start petalinux config. This will set correct temporary path variable.

7. Add Linux files (bl31.elf, uboot.elf and image.ub) to prebuilt folder
   a. "prebuilt\os\petalinux\default" or "prebuilt\os\petalinux\<short name>"
      Notes: Scripts select "prebuilt\os\petalinux\<short name>", if exist, otherwise "prebuilt\os\petalinux\default"

8. Generate Programming Files with HSI/SDK
   a. Run on Vivado TCL: TE::sw_run_hsi
      Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
   b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk
      Note: See SDK Projects\(^{10}\)

---

\(^9\) https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart
\(^{10}\) https://wiki.trenz-electronic.de/display/PD/SDK+Projects
6 Launch

### 6.1 Programming

- Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging](https://wiki.trenz-electronic.de/pages/viewpage.action?pageId=14746264#Vivado/SDK/SDSoC-XilinxSoftwareProgrammingandDebugging)

#### 6.1.1 QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp u-boot
   - Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup
   - optional "TE::pr_program_flash_binfile -swapp hello_te0803" possible
4. Copy image.ub on SD-Card
5. Insert SD-Card

#### 6.1.2 SD

1. Copy image.ub and Boot.bin on SD-Card.
   - For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Set Boot Mode to SD-Boot.
3. Insert SD-Card in SD-Slot.

#### 6.1.3 JTAG

Not used on this Example.

### 6.2 Usage

1. Prepare HW like described on section Programming (see page 17)
2. Connect UART USB (JTAG XMOD)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)
   - Note: See TRM of the Carrier, which is used.
4. (Optional) Insert PCIe Card (detection depends on Linux driver. Only some basic drivers are installed)
5. (Optional) Connect Sata Disc
7. (Optional) Connect Network Cable

---

8. Power On PCB
   Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from SD into OCM, 2. FSBL loads ATF(bl31.elf) and U-boot from SD/QSPI into DDR, 3. U-boot load Linux from SD into DDR.

6.2.1 Linux

1. Open Serial Console (e.g. putty)
   a. Speed: 115200
   b. COM Port: Win OS, see device manager, Linux OS see `dmesg |grep tty` (UART is *USB1)

2. Linux Console:
   Note: Wait until Linux boot finished For Linux Login use:
   a. User Name: root
   b. Password: root

3. You can use Linux shell now.
   a. I2C 0 Bus type: `i2cdetect -y -r 0`
   b. ETH0 works with udhcpc
   c. USB type "lsusb" or connect USB device
   d. PCIe type "lspci"

6.2.2 Vivado Hardware Manager

Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).

• GPIO Interface:
  • Set Enable to send Write data over RGPIO interface.
    • Important, see description to set correct values: TEBF0808 Master CPLD\(^{12}\), TEBF0808 Slave CPLD\(^{13}\)

• LED Control +CAN+S:
  • XMOD 2(without green dot) and HD LED are accessible.

---
\(^{12}\) https://wiki.trenz-electronic.de/display/PD/TEBF0808+Master+CPLD\#TEBF0808MasterCPLD-RGPIO
\(^{13}\) https://wiki.trenz-electronic.de/display/PD/TEBF0808+Slave+CPLD\#TEBF0808SlaveCPLD-RGPIO
Hardware

- localhost (1)
  - Connected
  - Open
- other_board (2)
  - Programmed

System Monitor

- hw_vio_1
  - Status: OK - Outputs 1
- hw_vio_2
  - Status: OK - Outputs 2
- arm_depl (1)
  - Status: NOT

System Monitor

- hw_vio

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Activity</th>
<th>Direction</th>
<th>pin</th>
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<td>[B10]</td>
<td>☑️</td>
<td>Output</td>
<td>hw_vio_1</td>
</tr>
<tr>
<td>a5_vio_CFG2</td>
<td>[H: 0O_0000]</td>
<td>☑️</td>
<td>Output</td>
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<tr>
<td>a5_vio_CFG3</td>
<td>[H: 0O_0000]</td>
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<td>[H: FF_51C]</td>
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<td>hw_vio_1</td>
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<tr>
<td>a5_vio_CFG5</td>
<td>[H: FF_51C]</td>
<td>☑️</td>
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<td>hw_vio_1</td>
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</table>
7 System Design - Vivado

7.1 Block Design

7.1.1 PS Interfaces

Activated interfaces:

<table>
<thead>
<tr>
<th>Type</th>
<th>Note</th>
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<tbody>
<tr>
<td>DDR</td>
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<tr>
<td>QSPI</td>
<td>MIO</td>
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<td>MIO</td>
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<td>SD1</td>
<td>MIO</td>
</tr>
<tr>
<td>CAN0</td>
<td>EMIO</td>
</tr>
<tr>
<td>I2C0</td>
<td>MIO</td>
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<tr>
<td>PJTAG0</td>
<td>MIO</td>
</tr>
<tr>
<td>UART0</td>
<td>MIO</td>
</tr>
<tr>
<td>GPIO0</td>
<td>MIO</td>
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<tr>
<td>SWDT0..1</td>
<td>MIO</td>
</tr>
<tr>
<td>Type</td>
<td>Note</td>
</tr>
<tr>
<td>--------------</td>
<td>-----------</td>
</tr>
<tr>
<td>TTC0..3</td>
<td>MIO</td>
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<tr>
<td>GEM3</td>
<td>MIO</td>
</tr>
<tr>
<td>USB0</td>
<td>MIO/GTP</td>
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<tr>
<td>PCIe</td>
<td>MIO/GTP</td>
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<tr>
<td>SATA</td>
<td>GTP</td>
</tr>
<tr>
<td>DisplayPort</td>
<td>EMIO/GTP</td>
</tr>
</tbody>
</table>

7.2 Constrain

7.2.1 Basic module constrain

```bash
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```
7.2.2 Design specific constrain

```
_i_io.xdc

# system controller ip
#LED_HD SC0 J3:31
#LED_XMOD SC17 J3:48
#CAN_RX SC19 J3:52 B26_L11_P
#CAN_TX SC18 J3:50 B26_L11_N
#CAN_S SC16 J3:46 B26_L1_N

set_property PACKAGE_PIN G14 [get_ports BASE_sc0]
set_property PACKAGE_PIN D15 [get_ports BASE_sc5]
set_property PACKAGE_PIN H13 [get_ports BASE_sc6]
set_property PACKAGE_PIN H14 [get_ports BASE_sc7]
set_property PACKAGE_PIN A13 [get_ports BASE_sc10_io]
set_property PACKAGE_PIN B13 [get_ports BASE_sc11]
set_property PACKAGE_PIN A14 [get_ports BASE_sc12]
set_property PACKAGE_PIN B14 [get_ports BASE_sc13]
set_property PACKAGE_PIN F13 [get_ports BASE_sc14]
set_property PACKAGE_PIN G13 [get_ports BASE_sc15]
set_property PACKAGE_PIN A15 [get_ports BASE_sc16]
set_property PACKAGE_PIN B15 [get_ports BASE_sc17]
set_property PACKAGE_PIN J14 [get_ports BASE_sc18]
set_property PACKAGE_PIN K14 [get_ports BASE_sc19]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc0]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc5]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc6]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc7]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc10_io]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc11]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc12]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc13]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc14]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc15]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc16]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc17]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc18]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc19]

# Audio Codec
#LRCLK          J3:49
#BCLK           J3:51
#DAC_SDATA      J3:53
#ADC_SDATA      J3:55
set_property PACKAGE_PIN L13 [get_ports LRCLK]
set_property PACKAGE_PIN L14 [get_ports BCLK]
set_property PACKAGE_PIN E15 [get_ports DAC_SDATA]
set_property PACKAGE_PIN F15 [get_ports ADC_SDATA]
set_property IOSTANDARD LVCMOS18 [get_ports LRCLK]
set_property IOSTANDARD LVCMOS18 [get_ports BCLK]
set_property IOSTANDARD LVCMOS18 [get_ports DAC_SDATA]
```

http://www.trenz-electronic.de
set_property IOSTANDARD LVCMOS18 [get_ports ADC_SDATA]
8 Software Design - SDK/HSI

For SDK project creation, follow instructions from:  
SDK Projects

8.1 Application

SDK template in ./sw_lib/sw_apps/ available.

8.1.1 zynqmp_fsbl

TE modified 2018.2 FSBL

Changes:
- Si5338 Configuration, PCIe Reset over GPIO
  - see xfsbl_board.c and xfsbl_board.h, xfsbl_main.c
- Add register_map.h, si5338.c, si5338.h

Note: Remove compiler flags "-Os -flto -ffat-lto-objects" on 2018.2 SDK to generate FSBL

8.1.2 zynqmp_fsbl_flash

TE modified 2018.2 FSBL

Changes:
- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation

Note: Remove compiler flags "-Os -flto -ffat-lto-objects" on 2018.2 SDK to generate FSBL

8.1.3 zynqmp_pmufw

Xilinx default PMU firmware.

8.1.4 hello_te0803

Hello TE0803 is a Xilinx Hello World example as endless loop instead of one console output.

8.1.5 u-boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.

14 https://wiki.trenz-electronic.de/display/PD/SDK+Projects
9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

9.1 Config

Activate:

- SUBSYSTEM_PRIMARY_SD_PSU_SD_1_SELECT

9.2 U-Boot

- Change platform-top.h

```c
#include <configs/platform-auto.h>
#define CONFIG_SYS_BOOTM_LEN 0xF000000

#define DFU_ALT_INFO_RAM "dfu_ram_info="
     "setenv dfu_alt_info "
    "image.ub ram $netstart 0x1e00000\0"
    "dfu_ram=run dfu_ram_info && dfu 0 ram 0\0"
    "thor_ram=run dfu_ram_info && thordown 0 ram 0\0"

#define DFU_ALT_INFO_MMC "dfu_mmc_info="
    "$\{kernel_image\} fat 0 1\\;"
    "dfu_mmc=run dfu_mmc_info && dfu 0 mmc 0\0"
    "thor_mmc=run dfu_mmc_info && thordown 0 mmc 0\0"

/*Required for uartless designs */
#ifndef CONFIG_BAUDRATE
#define CONFIG_BAUDRATE 115200
#endif CONFIG_DEBUG_UART
#endif CONFIG_DEBUG_UART
#endif
#endif

/*Define CONFIG_ZYNQMP_EEPROM here and its necessaries in u-boot menuconfig if you had EEPROM memory. */
#ifndef CONFIG_ZYNQMP_EEPROM
#define CONFIG_SYS_I2C_EEPROM_ADDR_LEN 1
#define CONFIG_CMD_EEPROM
#define CONFIG_ZYNQ_EEPROM_BUS 5
#define CONFIG_ZYNQ_GEM_EEPROM_ADDR 0x54
#define CONFIG_ZYNQ_GEM_I2C_MAC_OFFSET 0x20
#endif
```

15 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart
9.3 Device Tree

```
/include/ "system-conf.dtsi"
/

/* default */
/* SD */

&sdhci1 {
    // disable-wp;
    no-1-8-v;
};

/* USB */

&dwc3_0 {
    status = "okay";
    dr_mode = "host";
};

/* ETH PHY */

&gem3 {
    phy-handle = <&phy0>
    phy0: phy0@1 {
        device_type = "ethernet-phy";
        reg = <1>
    }
};

/* QSPI */

&qspi {
    #address-cells = <1>
    #size-cells = <0>
    status = "okay"
    flash0: flash0@0 {
        compatible = "jedec,spi-nor"
        reg = <0x0>
        #address-cells = <1>
        #size-cells = <1>
    }
};

/* I2C */

&i2c0 {
    i2cswitch@73 {
        compatible = "nxp,pca9548"
        #address-cells = <1>
    }
};
```
#size-cells = <0>;  
reg = <0x73>;  
i2c-mux-idle-disconnect;

i2c@2 { // PCIe  
    #address-cells = <1>;  
    #size-cells = <0>;  
    reg = <2>;  
};  
i2c@3 { // i2c SFP  
    #address-cells = <1>;  
    #size-cells = <0>;  
    reg = <3>;  
};  
i2c@4 { // i2c SFP  
    #address-cells = <1>;  
    #size-cells = <0>;  
    reg = <4>;  
};  
i2c@5 { // i2c EEPROM  
    #address-cells = <1>;  
    #size-cells = <0>;  
    reg = <5>;  
};  
i2c@6 { // i2c FMC  
    #address-cells = <1>;  
    #size-cells = <0>;  
    reg = <6>;  
};  

si570_2: clock-generator3@5d {  
    #clock-cells = <0>;  
    compatible = "silabs,si570";  
    reg = <0x5d>;  
    temperature-stability = <50>;  
    factory-fout = <156250000>;  
    clock-frequency = <78800000>;  
};  
i2c@7 { // i2c USB HUB  
    #address-cells = <1>;  
    #size-cells = <0>;  
    reg = <7>;  
};  

i2c-switch@77 { // u  
    compatible = "nxp, pca9548";  
    #address-cells = <1>;  
    #size-cells = <0>;  
    reg = <0x77>;  
    i2c-mux-idle-disconnect;  
};  
i2c@0 { // i2c PMOD  
    #address-cells = <1>;  
    #size-cells = <0>;  
    reg = <0>;  
};  
i2c@1 { // i2c Audio Codec
#address-cells = <1>;  
#size-cells = <0>;  
reg = <1>;  
/*
adau1761: adau1761@38 {
    compatible = "adi,adau1761";
    reg = <0x38>;
}; */

i2c@2 { // i2c FireFly A
    #address-cells = <1>;  
    #size-cells = <0>;  
    reg = <2>;
};

i2c@3 { // i2c FireFly B
    #address-cells = <1>;  
    #size-cells = <0>;  
    reg = <3>;
};

i2c@4 { // i2c PLL
    #address-cells = <1>;  
    #size-cells = <0>;  
    reg = <4>;
};

i2c@5 { // i2c SC
    #address-cells = <1>;  
    #size-cells = <0>;  
    reg = <5>;
};

i2c@6 { // i2c
    #address-cells = <1>;  
    #size-cells = <0>;  
    reg = <6>;
};

i2c@7 { // i2c
    #address-cells = <1>;  
    #size-cells = <0>;  
    reg = <7>;
};

/ * UNUSED DMA disable */

&lpd_dma_chan1 {
    status = "disabled";
};

&lpd_dma_chan2 {
    status = "disabled";
};

&lpd_dma_chan3 {
    status = "disabled";
};

&lpd_dma_chan4 {
    status = "disabled";
};
9.4 Kernel

Deactivate:
- CONFIG_CPU_IDLE   (only needed to fix JTAG Debug issue)
- CONFIG_CPU_FREQ   (only needed to fix JTAG Debug issue)

9.5 Rootfs

Activate:
- i2c-tools

9.6 Applications

9.6.1 startup

Script App to load init.sh from SD Card if available.
See: os\petalinux\project-spec\meta-user\recipes-apps\startup\files
10 Additional Software

10.1 SI5338

Download ClockBuilder Desktop for SI5338

1. Install and start ClockBuilder
2. Select SI5338
3. Options → Open register map file
   Note: File location <design name>/misc/SI5338/RegisterMap.txt
4. Modify settings
5. Options → save C code header files
6. Replace Header files from FSBL template with generated file

---

16 https://www.silabs.com/products/development-tools/software/clock
## 11 Appx. A: Change History and Legal Notices

### 11.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

<table>
<thead>
<tr>
<th>Date</th>
<th>Document Revision</th>
<th>Authors</th>
<th>Description</th>
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<td>2018-10-26</td>
<td>v.21</td>
<td>John Hartfiel</td>
<td>• new assembly variant</td>
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<td>14.08.2018</td>
<td>v.19</td>
<td>John Hartfiel</td>
<td>• design update</td>
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17 https://wiki.trenz-electronic.de/display/~j.hartfiel
18 https://wiki.trenz-electronic.de/display/~j.hartfiel
11.2 Legal Notices

11.3 Data privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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\(^{20}\) [https://echa.europa.eu/candidate-list-table](https://echa.europa.eu/candidate-list-table)