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Online version of this manual and other related documents can be found at https://wiki.trenz-electronic.de/display/PD/Trenz+Electronic+Documentation
4 Overview

Linux with basic periphery of TE0807 Starterkit (TEBF0808 Carrier).

4.1 Key Features

- TEBF0808
- Linux
- USB
- ETH
- PCIe
- SATA
- SD
- I2C
- DP
- RGPIO
- user LED access
- Modified FSBL for Si5345 programming
- Special FSBL for QSPI Programming

4.2 Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Vivado</th>
<th>Project Built</th>
<th>Authors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>TE0807-StarterKit-vivado_2018.2-build_04_20190207111616.zip</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2018-09-04</td>
<td>2018.2</td>
<td>TE0807-StarterKit_noprebuilt-vivado_2018.2-build_03_20180904122245.zip</td>
<td>John Hartfiel</td>
<td>small petalinux changes, IO renaming, PL Design changes, additional notes for FSBL generated with Win SDK, changed *.bif</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0807-StarterKit-vivado_2018.2-build_03_20180904121600.zip</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Date</td>
<td>Vivado</td>
<td>Project Built</td>
<td>Authors</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>--------</td>
<td>--------------------------------------------------------------------------------</td>
<td>--------------</td>
<td>--------------------------------------</td>
</tr>
<tr>
<td>2018-05-24</td>
<td>2017.4</td>
<td>TE0807-StarterKit_noprebuild-vivado_2017.4-build_10_20180524150124.zip</td>
<td>John Hartfiel</td>
<td>solved Linux Flash issue</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0807-StarterKit-vivado_2017.4-build_10_20180524150106.zip</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2018-02-06</td>
<td>2017.4</td>
<td>TE0807-StarterKit_noprebuild-vivado_2017.4-build_05_20180206082637.zip</td>
<td>John Hartfiel</td>
<td>same CLK for VIO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0807-StarterKit-vivado_2017.4-build_05_20180206082621.zip</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2018-02-05</td>
<td>2017.4</td>
<td>TE0807-StarterKit-vivado_2017.4-build_05_20180205101252.zip</td>
<td>John Hartfiel</td>
<td>solved JTAG/Linux issue</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0807-StarterKit_noprebuild-vivado_2017.4-build_05_20180205101306.zip</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2018-01-18</td>
<td>2017.4</td>
<td>TE0807-StarterKit_noprebuild-vivado_2017.4-build_05_20180118152938.zip</td>
<td>John Hartfiel</td>
<td>initial release</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0807-StarterKit-vivado_2017.4-build_05_20180118152922.zip</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
4.3 Release Notes and Know Issues

<table>
<thead>
<tr>
<th>Issues</th>
<th>Description</th>
<th>Workaround/Solution</th>
<th>To be fixed version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash access on Linux</td>
<td>Device tree is not correct on Linux</td>
<td>add compatibility to &quot;compatible &quot;jedec,spi-nor&quot;&quot;</td>
<td>Solved with 20180524 update</td>
</tr>
</tbody>
</table>
| USB UART Terminal is blocked / SDK Debugging is blocked | This happens only with 2017.4 Linux , when JTAG connection is established on Vivado HW Manager. | Do not use HW Manager connection, or if debugging is nessecary:  
1. Boot linux with usb terminal  
2. From the terminal: root root mount ifconfig eth0  
3. Open two new SSH terminals via ethernet: root root , run user application ...  
4. Exit and close the usb terminal | Solved with 20180205 update |

4.4 Requirements

4.4.1 Software

<table>
<thead>
<tr>
<th>Software</th>
<th>Version</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vivado</td>
<td>2018.2</td>
<td>needed</td>
</tr>
<tr>
<td>SDK</td>
<td>2018.2</td>
<td>needed</td>
</tr>
<tr>
<td>PetaLinux</td>
<td>2018.2</td>
<td>needed</td>
</tr>
</tbody>
</table>

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.¹  
Complete List is available on <design name>/board_files/*_board_files.csv

¹ https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files
Design supports following modules:

<table>
<thead>
<tr>
<th>Module Model</th>
<th>Board Part Short Name</th>
<th>PCB Revision Support</th>
<th>DDR</th>
<th>QSPI Flash</th>
<th>Others</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0807-01-ES2</td>
<td>es2_sk</td>
<td>REV01</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0807-02-07EV-1E</td>
<td>7ev_1e_sk</td>
<td>REV02</td>
<td>4GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: Design contains also Board Part Files for TE0807 only configuration, this board part files are not used for this reference design.

Design supports following carriers:

<table>
<thead>
<tr>
<th>Carrier Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEBF0808</td>
<td>Used as reference carrier.</td>
</tr>
</tbody>
</table>

Additional HW Requirements:

<table>
<thead>
<tr>
<th>Additional Hardware</th>
<th>Notes</th>
</tr>
</thead>
</table>

### 4.5 Content

For general structure and of the reference design, see [Project Delivery](https://wiki.trenz-electronic.de/display/PD/Project+Delivery)

### 4.5.1 Design Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vivado</td>
<td><code>&lt;design name&gt;/block_design</code></td>
<td>Vivado Project will be generated by TE Scripts</td>
</tr>
<tr>
<td></td>
<td><code>&lt;design name&gt;/constraints</code></td>
<td></td>
</tr>
<tr>
<td></td>
<td><code>&lt;design name&gt;/ip_lib</code></td>
<td></td>
</tr>
<tr>
<td>SDK/HSI</td>
<td><code>&lt;design name&gt;/sw_lib</code></td>
<td>Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI</td>
</tr>
<tr>
<td>PetaLinux</td>
<td><code>&lt;design name&gt;/os/petalinux</code></td>
<td>PetaLinux template with current configuration</td>
</tr>
</tbody>
</table>
4.5.2 Additional Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>SI5345</td>
<td>&lt;design name&gt;/misc/SI5345</td>
<td>SI5345 Project with current PLL Configuration</td>
</tr>
</tbody>
</table>

4.5.3 Prebuilt

<table>
<thead>
<tr>
<th>File</th>
<th>File-Extension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIF-File</td>
<td>*.bif</td>
<td>File with description to generate Bin-File</td>
</tr>
<tr>
<td>BIN-File</td>
<td>*.bin</td>
<td>Flash Configuration File with Boot-Image (Zynq-FPGAs)</td>
</tr>
<tr>
<td>BIT-File</td>
<td>*.bit</td>
<td>FPGA (PL Part) Configuration File</td>
</tr>
<tr>
<td>DebugProbes-File</td>
<td>*.ltx</td>
<td>Definition File for Vivado/Vivado Labtools Debugging Interface</td>
</tr>
<tr>
<td>Diverse Reports</td>
<td>---</td>
<td>Report files in different formats</td>
</tr>
<tr>
<td>Hardware-Platform-</td>
<td>*.hdf</td>
<td>Exported Vivado Hardware Specification for SDK/HSI and PetaLinux</td>
</tr>
<tr>
<td>Specification-Files</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LabTools Project-File</td>
<td>*.lpr</td>
<td>Vivado Labtools Project File</td>
</tr>
<tr>
<td>OS-Image</td>
<td>*.ub</td>
<td>Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)</td>
</tr>
<tr>
<td>Software-Application-File</td>
<td>*.elf</td>
<td>Software Application for Zynq or MicroBlaze Processor Systems</td>
</tr>
</tbody>
</table>

4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:
• TE0807 "StarterKit" Reference Design

3 https://shop.trez-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0807/Reference_Design/2018.2/StarterKit
5 Design Flow

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:
- Vivado/SDK/SDSoC
- Vivado Projects
- Project Delivery

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with ".create_win_setup.cmd" on Windows OS and ".create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Limits of functionality see: Project Delivery

1. "create_win_setup.cmd", "create_linux_setup.sh" and follow instructions on shell:

2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project
   a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
      Note: Select correct one, see TE Board Part Files
   b. Important: Use Board Part Files, which ends with *_tebf0808
5. Create HDF and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
      Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (bl31.elf, uboot.elf and image.ub) with exported HDF

---

5 https://wiki.trenz-electronic.de/display/PD/VivadoProjects
6 https://wiki.trenz-electronic.de/display/PD/ProjectDelivery
7 https://wiki.trenz-electronic.de/display/PD/ProjectDelivery#ProjectDelivery-Currentlylimitationsoffunctionality
8 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files
a. HDF is exported to "prebuilt\hardware\<short name>"
   Note: HW Export from Vivado GUI create another path as default workspace.

Create Linux images on VM, see PetaLinux KICKstart
   i. Use TE Template from /os/petalinux
      Note: run init_config.sh before you start petalinux config. This will set correct temporary path
      variable.

7. Add Linux files (bl31.elf, uboot.elf and image.ub) to prebuilt folder
   a. "prebuilt\os\petalinux\default" or "prebuilt\os\petalinux\<short name>"
      Notes: Scripts select "prebuilt\os\petalinux\<short name>", if exist, otherwise
      "prebuilt\os\petalinux\default"

8. Generate Programming Files with HSI/SDK
   a. Run on Vivado TCL: TE::sw_run_hsi
      Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
   b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk
      Note: See SDK Projects
6 Launch

6.1 Programming

⚠️ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

6.1.1 QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp u-boot
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup
   Optional "TE::pr_program_flash_binfile -swapp hello_te0807" possible
4. Copy image.ub on SD-Card
5. Insert SD-Card

6.1.2 SD

1. Copy image.ub and Boot.bin on SD-Card.
   • For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Set Boot Mode to SD-Boot.
3. Insert SD-Card in SD-Slot.

6.1.3 JTAG

Not used on this Example.

6.2 Usage

1. Prepare HW like described on section Programming (see page 15)
2. Connect UART USB (JTAG XMOD)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)
   Note: See TRM of the Carrier, which is used.
4. (Optional) Insert PCIe Card (detection depends on Linux driver. Only some basic drivers are installed)
5. (Optional) Connect Sata Disc
7. (Optional) Connect Network Cable

---

8. **Power On PCB**
   Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from SD into OCM, 2. FSBL loads ATF(bl31.elf) and U-boot from SD/QSPI into DDR, 3. U-boot load Linux from SD into DDR.

### 6.2.1 Linux

1. **Open Serial Console (e.g. putty)**
   a. Speed: 115200
   b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is "USB1")

2. **Linux Console:**
   Note: Wait until Linux boot finished For Linux Login use:
   a. User Name: root
   b. Password: root

3. **You can use Linux shell now.**
   a. I2C 0 Bus type: `i2cdetect -y -r 0`
   b. ETH0 works with `udhcpc`
   c. USB type "`lsusb`" or connect USB device
   d. PCIe type "`lspci`"

### 6.2.2 Vivado Hardware Manager

Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).

- **RGPIO Interface:**
  - Set Bit 31-28 to "1010" to activate RGPIO Interface of Master or Slave CPLD.
  - Description: [TEBF0808 Master CPLD](https://wiki.trenz-electronic.de/display/PD/TEBF0808+Master+CPLD#TEBF0808MasterCPLD-RGPIO), [TEBF0808 Slave CPLD](https://wiki.trenz-electronic.de/display/PD/TEBF0808+Slave+CPLD#TEBF0808SlaveCPLD-RGPIO)

- **LED Control:**
  - XMOD 2(without green dot) and HD LED are accessible.
7 System Design - Vivado

7.1 Block Design

7.1.1 PS Interfaces

Activated interfaces:

<table>
<thead>
<tr>
<th>Type</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR</td>
<td></td>
</tr>
<tr>
<td>QSPI</td>
<td>MIO</td>
</tr>
<tr>
<td>SD0</td>
<td>MIO</td>
</tr>
<tr>
<td>SD1</td>
<td>MIO</td>
</tr>
<tr>
<td>CAN0</td>
<td>EMIO</td>
</tr>
<tr>
<td>I2C0</td>
<td>MIO</td>
</tr>
<tr>
<td>PJTAG0</td>
<td>MIO</td>
</tr>
<tr>
<td>UART0</td>
<td>MIO</td>
</tr>
<tr>
<td>GPIO0</td>
<td>MIO</td>
</tr>
<tr>
<td>SWDT0..1</td>
<td></td>
</tr>
</tbody>
</table>
Type | Note  
---|---  
TTC0..3 |  
GEM3 | MIO  
USB0 | MIO/GTP  
PCIe | MIO/GTP  
SATA | GTP  

7.2 Constrains

7.2.1 Basic module constrains

```plaintext
_i_bitgen.xdc

set_property BITSTREAMGENERALCOMPRESSTRUE [current_design]
set_property BITSTREAMCONFIGUNUSEDPINPULLNONE [current_design]
```
7.2.2 Design specific constrain

_i.io.xdc

# System Controller IP

# J3:31 LED_HD
set_property PACKAGE_PIN K11 [get_ports BASE_sc0]
# J3:41
set_property PACKAGE_PIN E14 [get_ports BASE_sc5]
# J3:45
set_property PACKAGE_PIN C12 [get_ports BASE_sc6]
# J3:47
set_property PACKAGE_PIN D12 [get_ports BASE_sc7]
# J3:32
set_property PACKAGE_PIN J12 [get_ports BASE_sc10_io]
# J3:34
set_property PACKAGE_PIN K13 [get_ports BASE_sc11]
# J3:36
set_property PACKAGE_PIN A13 [get_ports BASE_sc12]
# J3:38
set_property PACKAGE_PIN A14 [get_ports BASE_sc13]
# J3:40
set_property PACKAGE_PIN E12 [get_ports BASE_sc14]
# J3:42
set_property PACKAGE_PIN F12 [get_ports BASE_sc15]
# J3:46 CAN S
set_property PACKAGE_PIN A12 [get_ports BASE_sc16]
# J3:48 LED_XMOD
set_property PACKAGE_PIN B12 [get_ports BASE_sc17]
# J3:50 CAN TX
set_property PACKAGE_PIN B14 [get_ports BASE_sc18]
# J3:52 CAN RX
set_property PACKAGE_PIN C14 [get_ports BASE_sc19]

set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc0]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc5]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc6]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc7]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc10_io]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc11]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc12]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc13]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc14]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc15]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc16]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc17]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc18]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc19]

# PLL
# J4:74
#set_property PACKAGE_PIN AF15 [get_ports {si570_clk_p[0]}]
#set_property IOSTANDARD LVDS [get_ports {si570_clk_p[0]}]
#set_property IOSTANDARD LVDS [get_ports {si570_clk_n[0]}]

# Audio Codec
#LRCLK J3:49 B47_L9_N
#BCLK J3:51 B47_L9_P
#DAC_SDATA J3:53 B47_L7_N
#ADC_SDATA J3:55 B47_L7_P
set_property PACKAGE_PIN G14 [get_ports LRCLK ]
set_property PACKAGE_PIN H14 [get_ports BCLK ]
set_property PACKAGE_PIN C13 [get_ports DAC_SDATA ]
set_property PACKAGE_PIN D14 [get_ports ADC_SDATA ]
set_property IOSTANDARD LVCMOS18 [get_ports LRCLK ]
set_property IOSTANDARD LVCMOS18 [get_ports BCLK ]
set_property IOSTANDARD LVCMOS18 [get_ports DAC_SDATA ]
set_property IOSTANDARD LVCMOS18 [get_ports ADC_SDATA ]
8 Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects\(^{14}\)

8.1 Application

 SDK template in ./sw_lib/sw_apps/ available.

8.1.1 FSBL

TE modified 2018.2 FSBL

Changes:

- Si5345Configuration, PCIe Reset over GPIO
- See xfsbl_board.c and xfsbl_board.h
- Add Si5345-Registers.h, si5345.c, si5345.h

Note: Remove compiler flags "-Os -flto -fflat-lto-objects" on 2018.2 SDK to generate FSBL

8.1.2 zynqmp_fsbl_flash

TE modified 2018.2 FSBL

Changes:

- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation

Note: Remove compiler flags "-Os -flto -fflat-lto-objects" on 2018.2 SDK to generate FSBL

8.1.3 PMU

Xilinx default PMU firmware.

8.1.4 hello_te0807

Hello TE0807 is a Xilinx Hello World example as endless loop instead of one console output.

8.1.5 u-noot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.

\(^{14}\) https://wiki.trenz-electronic.de/display/PD/SDK+Projects
9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

9.1 Config

No changes.

9.2 U-Boot

- Change platform-top.h

```c
#include <configs/platform-auto.h>
define CONFIG_SYS_BOOTH_LEN 0xF000000

define DFU_ALT_INFO_RAM 
    "dfu_ram_info" 
    "setenv dfu_alt_info " 
    "image.ub ram $netstart 0x1e00000\0" 
    "dfu_ram=run dfu_ram_info && dfu 0 ram 0\0" 
    "thor_ram=run dfu_ram_info && thordown 0 ram 0\0"

define DFU_ALT_INFO_MMC 
    "dfu_mmc_info" 
    "set dfu_alt_info " 
    "${kernel_image} fat 0 1\\;" 
    "dfu_mmc=run dfu_mmc_info && dfu 0 mmc 0\0" 
    "thor_mmc=run dfu_mmc_info && thordown 0 mmc 0\0"

/*Required for uartless designs */
 ifndef CONFIG_BAUDRATE
 define CONFIG_BAUDRATE 115200
 ifdef CONFIG_DEBUG_UART
 undef CONFIG_DEBUG_UART
 endif
 endif

/*Define CONFIG_ZYNQMP_EEPROM here and its necessaries in u-boot menuconfig if you had EEPROM memory. */
 ifndef CONFIG_ZYNQMP_EEPROM
 define CONFIG_SYS_I2C_EEPROM_ADDR_LEN 1
 define CONFIG_CMD_EEPROM
 define CONFIG_ZYNQ_EEPROM_BUS 5
 define CONFIG_ZYNQ_EEPROM_ADDR 0x54
 define CONFIG_ZYNQ_E2C_MAC_OFFSET 0x20
 endif
```

15 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart
9.3 Device Tree

```
#include/ "system-conf.dtsi"
/
/* default */
/* SD */
&sdhci1 {
   // disable-wp;
   no-1-8-v;
};
/* USB */
&dwc3_0 {
   status = "okay";
   dr_mode = "host";
};
/* ETH PHY */
&gem3 {
   phy-handle = <&phy0>;
   phy0: phy0@1 {
      device_type = "ethernet-phy";
      reg = <1>;
   };
};
/* QSPI */
&qspi {
   #address-cells = <1>;
   #size-cells = <0>;
   status = "okay";
   flash0: flash0@0 {
      compatible = "jedec,spi-nor";
      reg = <0x0>;
      #address-cells = <1>;
      #size-cells = <1>;
   };
};
/* I2C */
&i2c0 {
   i2cswitch@73 { // u
      compatible = "nxp,pca9548";
      #address-cells = <1>;
```
#size-cells = <0>
reg = <0x73>
i2c-mux-idle-disconnect;

i2c@2 { // PCIe
    #address-cells = <1>
    #size-cells = <0>
    reg = <2>
};
i2c@3 { // i2c SFP
    #address-cells = <1>
    #size-cells = <0>
    reg = <3>
};
i2c@4 { // i2c SFP
    #address-cells = <1>
    #size-cells = <0>
    reg = <4>
};
i2c@5 { // i2c EEPROM
    #address-cells = <1>
    #size-cells = <0>
    reg = <5>
};
i2c@6 { // i2c FMC
    #address-cells = <1>
    #size-cells = <0>
    reg = <6>
};

si570_2: clock-generator3@5d {
    #clock-cells = <0>
    compatible = "silabs,si570"
    reg = <0x5d>
    temperature-stability = <50>
    factory-fout = <156250000>
    clock-frequency = <78800000>
};
i2c@7 { // i2c USB HUB
    #address-cells = <1>
    #size-cells = <0>
    reg = <7>
};

i2cswitch@77 { // u
    compatible = "nxp, pca9548"
    #address-cells = <1>
    #size-cells = <0>
    reg = <0x77>
    i2c-mux-idle-disconnect;
}
i2c@0 { // i2c PMOD
    #address-cells = <1>
    #size-cells = <0>
    reg = <0>
};
i2c@1 { // i2c Audio Codec
#address-cells = <1>;
#size-cells = <0>;
reg = <1>;
/*
adau1761: adau1761@38 {
    compatible = "adi,adau1761";
    reg = <0x38>;
};
*/
}

i2c@2 { // i2c FireFly A
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <2>;
};
i2c@3 { // i2c FireFly B
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <3>;
};
i2c@4 { // i2c PLL
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <4>;
};
i2c@5 { // i2c SC
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <5>;
};
i2c@6 { // i2c
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <6>;
};
i2c@7 { // i2c
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <7>;
};
/* UNUSED DMA disable */
&lpd_dma_chan1 {
    status = "disabled";
};
&lpd_dma_chan2 {
    status = "disabled";
};
&lpd_dma_chan3 {
    status = "disabled";
};
&lpd_dma_chan4 {
    status = "disabled";
9.4 Kernel

Deactivate:

- CONFIG_CPU_IDLE (only needed to fix JTAG Debug issue)
- CONFIG_CPU_FREQ (only needed to fix JTAG Debug issue)

9.5 Rootfs

Activate:

- i2c-tools

9.6 Applications

9.6.1 startup

Script App to load init.sh from SD Card if available.

See: \os\petalinux\project-spec\meta-user\recipes-apps\startup\files

9.6.2 adau1761init

Audio initialisation.
10 Additional Software

10.1 SI5345

Download ClockBuilder Pro for SI5345\textsuperscript{16}

1. Install and start ClockBuilder
2. Open "/misc/SI5345/Si5345-RevB-0807-02A-Project.slabtimeproj"
3. Modify settings
4. Export \rightarrow Register File \rightarrow select C code header \rightarrow save to file
5. Replace Header files from FSBL template with generated file

\textsuperscript{16} https://www.silabs.com/products/development-tools/software/clock
## Appx. A: Change History and Legal Notices

### 11.1 Document Change History

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<td>2019-02-07</td>
<td>v.15 (see page 6)</td>
<td>John Hartfiel</td>
<td>• new assembly variant</td>
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<tr>
<td>04.09.2018</td>
<td>v.13</td>
<td>John Hartfiel</td>
<td>• Release 2018.2</td>
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<tr>
<td>20.07.2018</td>
<td>v.12</td>
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<td>• Design update</td>
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<td>30.04.2018</td>
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<td>• Update known issues</td>
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<td>• Design update</td>
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17 [https://wiki.trenz-electronic.de/display/~j.hartfiel](https://wiki.trenz-electronic.de/display/~j.hartfiel)  
18 [https://wiki.trenz-electronic.de/display/~j.hartfiel](https://wiki.trenz-electronic.de/display/~j.hartfiel)
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\(^{19}\) http://guidance.eca.europa.eu/
\(^{20}\) https://eca.europa.eu/candidate-list-table
\(^{21}\) http://www.eca.europa.eu/
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