Online version of this document:
https://wiki.trenz-electronic.de/display/PD/TE0807+Test+Board

TE0807 Test Board

Revision v.9
Exported on 2019-05-06
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2 Table of Figures
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Online version of this manual and other related documents can be found at https://wiki.trenz-electronic.de/display/PD/Trenz+Electronic+Documentation
4 Overview

Design Example with minimum PS Setup (DDR, QSPI, UART0) only for custom boards or easier debug via SDK.

4.1 Key Features

- QSPI
- SDK
- Custom Carrier (minimum PS Design with available module components only)
- Special FSBL for QSPI Programming

4.2 Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Vivado</th>
<th>Project Built</th>
<th>Authors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2019-02-08</td>
<td>2018.2</td>
<td>TE0807-test_board_noprebuilt-vivado_2018.2-build_04_20190207111539.zip</td>
<td>John Hartfiel</td>
<td>• new assembly variant</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0807-test_board-vivado_2018.2-build_04_20190207111524.zip</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2018-09-04</td>
<td>2018.2</td>
<td>TE0807-test_board_noprebuilt-vivado_2018.2-build_03_20180904121458.zip</td>
<td>John Hartfiel</td>
<td>• additional notes for FSBL generated with Win SDK</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0807-test_board-vivado_2018.2-build_03_20180904121522.zip</td>
<td></td>
<td>• changed *.bif</td>
</tr>
</tbody>
</table>
### 4.3 Release Notes and Known Issues

<table>
<thead>
<tr>
<th>Issues</th>
<th>Description</th>
<th>Workaround</th>
<th>To be fixed version</th>
</tr>
</thead>
<tbody>
<tr>
<td>No known issues</td>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
</tbody>
</table>

### 4.4 Requirements

#### 4.4.1 Software

<table>
<thead>
<tr>
<th>Software</th>
<th>Version</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vivado</td>
<td>2017.8</td>
<td>needed</td>
</tr>
<tr>
<td>SDK</td>
<td>2017.8</td>
<td>needed</td>
</tr>
</tbody>
</table>

#### 4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.¹

¹ [https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files](https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files)
Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

<table>
<thead>
<tr>
<th>Module Model</th>
<th>Board Part Short Name</th>
<th>PCB Revision Support</th>
<th>DDR</th>
<th>QSPI Flash</th>
<th>Others</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0807-01-ES2</td>
<td>es2</td>
<td>REV01</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0807-02-07EV-1E</td>
<td>7ev_1e</td>
<td>REV02</td>
<td>4GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: Design contains also Board Part Files for TE0807+TEBF0808 configuration, this board part files are not used for this reference design.

Design supports following carriers:

<table>
<thead>
<tr>
<th>Carrier Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Custom PCB</td>
<td>use simple Board Part files, if MIO connected is different to TEBF0808</td>
</tr>
<tr>
<td>TEBF0808</td>
<td>Used as reference carrier.</td>
</tr>
<tr>
<td>TEBT0808</td>
<td>Change UART0 to UART1 (MIO68...69) and regenerate design</td>
</tr>
</tbody>
</table>

Additional HW Requirements:

### Additional Hardware

**4.5 Content**

For general structure and of the reference design, see [Project Delivery](https://wiki.trenz-electronic.de/display/PD/Project+Delivery)

### 4.5.1 Design Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vivado</td>
<td>&lt;design name&gt;/block_design  &lt;design name&gt;/constraints &lt;design name&gt;/ip_lib</td>
<td>Vivado Project will be generated by TE Scripts</td>
</tr>
<tr>
<td>SDK/HSI</td>
<td>&lt;design name&gt;/sw_lib</td>
<td>Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI</td>
</tr>
</tbody>
</table>
4.5.2 Additional Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
</table>

4.5.3 Prebuilt

<table>
<thead>
<tr>
<th>File</th>
<th>File-Extension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIF-File</td>
<td>*.bif</td>
<td>File with description to generate Bin-File</td>
</tr>
<tr>
<td>BIN-File</td>
<td>*.bin</td>
<td>Flash Configuration File with Boot-Image (Zynq-FPGAs)</td>
</tr>
<tr>
<td>BIT-File</td>
<td>*.bit</td>
<td>FPGA (PL Part) Configuration File</td>
</tr>
<tr>
<td>Diverse Reports</td>
<td>---</td>
<td>Report files in different formats</td>
</tr>
<tr>
<td>Hardware-Platform-Specification-Files</td>
<td>*.hdf</td>
<td>Exported Vivado Hardware Specification for SDK/HSI and PetaLinux</td>
</tr>
<tr>
<td>LabTools Project-File</td>
<td>*.lpr</td>
<td>Vivado Labtools Project File</td>
</tr>
<tr>
<td>Software-Application-File</td>
<td>*.elf</td>
<td>Software Application for Zynq or MicroBlaze Processor Systems</td>
</tr>
</tbody>
</table>

4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0807 "Test Board" Reference Design³

5 Design Flow

Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:
- Vivado/SDK/SDSoC
- Vivado Projects
- Project Delivery

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:<design name>)
4. Create Project
   a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
   Note: Select correct one, see TE Board Part Files
   
   Important: Use Board Part Files, which did not ends with _tebf0808
5. Create HDF and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design-export_prebuilt
      Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Generate Programming Files with HSI/SDK

---

5 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects
6 https://wiki.trenz-electronic.de/display/PD/Project+Delivery
7 https://wiki.trenz-electronic.de/display/PD/Project+Delivery#ProjectDelivery-Currentlylimitationsoffunctionality
8 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files
a. Run on Vivado TCL: `TE::sw_run_hsi`
   Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: `TE::sw_run_sdk`
   Note: See SDK Projects⁹

⁹ https://wiki.trenz-electronic.de/display/PD/SDK+Projects
6 Launch

6.1 Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging](https://wiki.trenz-electronic.de/display/PD/SDK+Projects)

6.1.1 QSPI

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp hello_te0807
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup

Use SDK instead of Vivado is also possible, see: [SDK Projects#Xilinx%22HelloWorld%22onZynqMP](https://wiki.trenz-electronic.de/display/PD/SDK+Projects#SDKProjects-DebugSoftwareApplication)

6.1.2 SD

This does not work, because SD controller is not selected on PS.

6.1.3 JTAG

Load configuration and Application with SDK Debugger into device, see:

- [SDK Projects](https://wiki.trenz-electronic.de/display/PD/SDK+Projects)
- [SDK Projects](https://wiki.trenz-electronic.de/display/PD/SDK+Projects#SDKProjects-DebugSoftwareApplication)

6.2 Usage

QSPI Boot:

1. Prepare HW like described on section Programming (see page 13)
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI Card as Boot Mode
   Note: See TRM of the Carrier, which is used.
4. Power On PCB
   Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from QSPI into OCM, 2. FSBL loads Application into DDR

Debugging:

---

11 [https://wiki.trenz-electronic.de/display/PD/SDK+Projects#SDKProjects#Xilinx"HelloWorld"onZynqMP](https://wiki.trenz-electronic.de/display/PD/SDK+Projects#SDKProjects#Xilinx"HelloWorld"onZynqMP)
- [SDK Projects]¹⁴
- [SDK Projects]¹⁵

¹⁴ https://wiki.trenz-electronic.de/display/PD/SDK+Projects
¹⁵ https://wiki.trenz-electronic.de/display/PD/SDK+Projects#SDKProjects-DebugSoftwareApplication
7 System Design - Vivado

7.1 Block Design

### 7.1.1 PS Interfaces

Activated interfaces:

<table>
<thead>
<tr>
<th>Type</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR</td>
<td></td>
</tr>
<tr>
<td>QSPI</td>
<td>MIO</td>
</tr>
<tr>
<td>UART0</td>
<td>MIO, please select other one, if you have connected uart to second controller or other MIO</td>
</tr>
<tr>
<td>SWDT0..1</td>
<td></td>
</tr>
<tr>
<td>TTC0..3</td>
<td></td>
</tr>
</tbody>
</table>
7.2 Constrains

7.2.1 Basic module constrains

```
_i_bitgen.xdc

set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

7.2.2 Design specific constrain

Not needed.
8 Software Design - SDK/HSI

For SDK project creation, follow instructions from:
SDK Projects\textsuperscript{16}

8.1 Application

Template location: ./sw\lib/sw_apps/

8.1.1 zynqmp_fsbl

Xilinx default FSBL

8.1.2 zynqmp_fsbl_flash

TE modified 2017.4 FSBL

Changes:

- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation

8.1.3 hello_te0807

Hello TE0807 is a Xilinx Hello World example as endless loop instead of one console output.

---

\textsuperscript{16} https://wiki.trenz-electronic.de/display/PD/SDK+Projects
9 Additional Software

No additional software is needed.
10 Appx. A: Change History and Legal Notices

10.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

<table>
<thead>
<tr>
<th>Date</th>
<th>Document Revision</th>
<th>Authors</th>
<th>Description</th>
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<tr>
<td>2019-02-07</td>
<td>v.9 (see page 6)</td>
<td>John Hartfiel</td>
<td>• new assembly variant</td>
</tr>
<tr>
<td>04.09.2018</td>
<td>v.7</td>
<td>John Hartfiel</td>
<td>• Release 2018.2</td>
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<tr>
<td>2018-02-08</td>
<td>v.5</td>
<td>John Hartfiel</td>
<td>• Release 2017.4</td>
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<td>2017-11-14</td>
<td>v.3</td>
<td>John Hartfiel</td>
<td>• Release 2017.2</td>
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<tr>
<td>All</td>
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<td>John Hartfiel</td>
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</tr>
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</table>

10.2 Legal Notices

10.3 Data privacy

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17 https://wiki.trenz-electronic.de/display/~j.hartfiel
18 https://wiki.trenz-electronic.de/display/~j.hartfiel
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WEEE

\(^{19}\) http://guidance.echa.europa.eu/
\(^{20}\) https://echa.europa.eu/candidate-list-table
\(^{21}\) http://www.echa.europa.eu/

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