# Table of Contents

Overview ................................................................. 4  
Key Features .......................................................... 4  
Revision History ....................................................... 4  
Release Notes and Know Issues .................................... 4  
Requirements ................................................................ 4  
  Software .................................................................. 4  
  Hardware .................................................................. 5  
Content ...................................................................... 5  
  Design Sources ....................................................... 6  
  Additional Sources .................................................. 6  
  Prebuilt .................................................................. 6  
  Download .................................................................. 6  
Design Flow ............................................................... 7  
Launch ...................................................................... 9  
Programming .............................................................. 9  
  QSPI .................................................................... 9  
  SD ....................................................................... 9  
  JTAG .................................................................... 9  
Usage ...................................................................... 9  
System Design - Vivado .............................................. 11  
Block Design ............................................................. 11  
  PS Interfaces .......................................................... 11  
Constrains ................................................................. 11  
  Basic module constrains ........................................... 11  
  Design specific constrain .......................................... 11  
Software Design - SDK/HSI ......................................... 12  
Application ............................................................... 12  
  FSBL ................................................................... 12  
  Hello TE0808 ........................................................ 12  
Additional Software ................................................... 13  
Appx. A: Change History and Legal Notices ...................... 14  
  Document Change History ....................................... 14  
  Legal Notices ......................................................... 14  
  Data privacy ............................................................ 14  
  Document Warranty ............................................... 14  
  Limitation of Liability .............................................. 15  
  Copyright Notice .................................................... 15  
  Technology Licenses ............................................... 15  
  Environmental Protection ........................................ 15  
  REACH, RoHS and WEEE ......................................... 16
Online version of this manual and other related documents can be found at https://wiki.trenz-electronic.de/display/PD/Trenz+Electronic+Documentation
Overview

Design Example with minimum PS Setup (DDR, QSPI, UART0) only for custom boards or easier debug via SDK.

Key Features

- QSPI
- SDK
- Custom Carrier (with other MIO settings as TEBF0808)

Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Vivado</th>
<th>Project Built</th>
<th>Authors</th>
<th>Description</th>
</tr>
</thead>
</table>
| 2017-12-20 | 2017.2 | TE0808-test_board-vivado_2017.2-build_07_20171220192501.zip  
              TE0808-test_board_noprebuilt-vivado_2017.2-build_07_20171220192448.zip | John Hartfiel | Update Board Part Files                                                      |
| 2017-11-22 | 2017.2 | TE0808-test_board-vivado_2017.2-build_05_20171122080211.zip  
              TE0808-test_board_noprebuilt-vivado_2017.2-build_05_20171122080228.zip | John Hartfiel | Update Board Part CSV File  
                                                                          Regenerate design                      |
| 2017-11-16 | 2017.2 | TE0808-test_board-vivado_2017.2-build_05_20171116151545.zip  
              TE0808-test_board_noprebuilt-vivado_2017.2-build_05_20171116151600.zip | John Hartfiel | Update Board Part CSV File with new Flash assembly variants                 |
| 2017-11-13 | 2017.2 | TE0808-test_board-vivado_2017.2-build_05_2017113140954.zip  
              TE0808-test_board_noprebuilt-vivado_2017.2-build_05_2017113141908.zip | John Hartfiel | initial release                                                             |

Release Notes and Know Issues

<table>
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<tr>
<th>Issues</th>
<th>Description</th>
<th>Workaround</th>
<th>To be fixed version</th>
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<tr>
<td>No known issues</td>
<td>--</td>
<td>--</td>
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Requirements

Software

<table>
<thead>
<tr>
<th>Software</th>
<th>Version</th>
<th>Note</th>
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<tbody>
<tr>
<td>Vivado</td>
<td>2017.2</td>
<td>needed</td>
</tr>
</tbody>
</table>
Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

<table>
<thead>
<tr>
<th>Module Model</th>
<th>Board Part Short Name</th>
<th>PCB Revision Support</th>
<th>DDR</th>
<th>QSPI Flash</th>
<th>Others</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0808-ES1</td>
<td>es1</td>
<td>REV02, REV03</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-ES2</td>
<td>es2</td>
<td>REV03, REV04</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-2ES2</td>
<td>2es2</td>
<td>REV03, REV04</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-1EA</td>
<td>9eg_1ea</td>
<td>REV04</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-1EB</td>
<td>9eg_1eb</td>
<td>REV04</td>
<td>4GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-1ED</td>
<td>9eg_1eb</td>
<td>REV04</td>
<td>4GB</td>
<td>64MB</td>
<td>2,5 mm connector</td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-1EE</td>
<td>9eg_1eb</td>
<td>REV04</td>
<td>4GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-1EL</td>
<td>9eg_1eb</td>
<td>REV04</td>
<td>4GB</td>
<td>128MB</td>
<td>2,5 mm connector</td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-2IB</td>
<td>9eg_2ib</td>
<td>REV04</td>
<td>4GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-2IE</td>
<td>9eg_2ib</td>
<td>REV04</td>
<td>4GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-15EG-1EB</td>
<td>15eg_1eb</td>
<td>REV04</td>
<td>4GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-15EG-1EE</td>
<td>15eg_1eb</td>
<td>REV04</td>
<td>4GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: Design contains also Board Part Files for TE0808+TEBF0808 configuration, this board part files are not used for this reference design. * Only different Flash size.

Design supports following carriers:

<table>
<thead>
<tr>
<th>Carrier Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Custom PCB</td>
<td>use simple Board Part files, if MIO connected is different to TEBF0808</td>
</tr>
<tr>
<td>TEBF0808</td>
<td>Used as reference carrier.</td>
</tr>
<tr>
<td>TEBT0808</td>
<td>Change UART0 to UART1 (MIO68...69) and regenerate design</td>
</tr>
</tbody>
</table>

Additional HW Requirements:

<table>
<thead>
<tr>
<th>Additional Hardware</th>
<th>Notes</th>
</tr>
</thead>
</table>

Content

For general structure and of the reference design, see Project Delivery
Design Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vivado</td>
<td><code>&lt;design name&gt;/block_design</code></td>
<td>Vivado Project will be generated by TE Scripts</td>
</tr>
<tr>
<td></td>
<td><code>&lt;design name&gt;/constraints</code></td>
<td></td>
</tr>
<tr>
<td></td>
<td><code>&lt;design name&gt;/ip_lib</code></td>
<td></td>
</tr>
<tr>
<td>SDK/HSI</td>
<td><code>&lt;design name&gt;/sw_lib</code></td>
<td>Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI</td>
</tr>
</tbody>
</table>

Additional Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
</table>

Prebuilt

<table>
<thead>
<tr>
<th>File</th>
<th>File-Extension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIF-File</td>
<td>*.bif</td>
<td>File with description to generate Bin-File</td>
</tr>
<tr>
<td>BIN-File</td>
<td>*.bin</td>
<td>Flash Configuration File with Boot-Image (Zynq-FPGAs)</td>
</tr>
<tr>
<td>BIT-File</td>
<td>*.bit</td>
<td>FPGA (PL Part) Configuration File</td>
</tr>
<tr>
<td>Diverse Reports</td>
<td>---</td>
<td>Report files in different formats</td>
</tr>
<tr>
<td>Hardware-Platform-Specification-Files</td>
<td>*.hdf</td>
<td>Exported Vivado Hardware Specification for SDK/HSI and PetaLinux</td>
</tr>
<tr>
<td>LabTools Project-File</td>
<td>*.lpr</td>
<td>Vivado Labtools Project File</td>
</tr>
<tr>
<td>Software-Application-File</td>
<td>*.elf</td>
<td>Software Application for Zynq or MicroBlaze Processor Systems</td>
</tr>
</tbody>
</table>

Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0808 Test Board
Design Flow

⚠️ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- Vivado/SDK/SDSoC/XilinxSoftware-BasicUserGuides
- Vivado Projects
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with ".create_win_setup.cmd" on Windows OS and ".create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. ".create_win_setup.cmd/.create_linux_setup.sh" and follow instructions on shell:

   ![Image](image_url)

   - Press 0 and enter for minimum setup
   - (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
   - Create Project
     a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
     Note: Select correct one, see TE Board Part Files
     Use Board Part Files, which did not ends with *_tebf0808
5. Create HDF and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
      Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is
      the same, except file export to prebuilt folder

6. Generate Programming Files with HSI/SDK
   a. Run on Vivado TCL: TE::sw_run_hsi
      Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.
      csv"
   b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::
      sw_run_sdk
      Note: See SDK Projects
Launch

Programming

⚠️ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

QSPI

1. Select JTAG as Boot Mode (see Carrier Description and ZynqMP TRM)
2. Connect JTAG to Host PC
3. Power On
4. Open Vivado Hardware Manager with Auto Connect
5. Right Click to FPGA Device XCU... and select Add Configuration Memory Device
   a. Select correct Flash Typ (see schematics or FPGAFLASH_TYP on test_board/board_files/TE0808_board_files.csv)
6. Open Program Configuration Memory Device
   a. Configuration file: test_board/prebuilt/boot_image/<short dir>/hello_te0808/Boot.bin
   b. Zynq FSBL: test_board/prebuilt/software/<short dir>/zynqmp_fsbl.elf
   c. Program Device Flash

Use SDK instead of Vivado is also possible, see: SDK Projects#Xilinx%22HelloWorld%22onZynqMP

SD

This does not work, because SD controller is not selected on PS.

JTAG

Load configuration and Application with SDK Debugger into device, see:

- SDK Projects
- SDK Projects#DebugSoftwareApplication

Usage

QSPI Boot:

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI Card as Boot Mode  
   Note: See TRM of the Carrier, which is used.

4. Power On PCB  
   Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from QSPI into OCM, 2. FSBL loads Application into DDR

Debugging:

- SDK Projects
- SDK Projects#DebugSoftwareApplication
System Design - Vivado

Block Design

PS Interfaces

Activated interfaces:

<table>
<thead>
<tr>
<th>Type</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR</td>
<td></td>
</tr>
<tr>
<td>QSPI</td>
<td>MIO</td>
</tr>
<tr>
<td>UART0</td>
<td>MIO, please select other one, if you have connected uart to second controller or other MIO</td>
</tr>
</tbody>
</table>

Constrains

Basic module constrains

```
.set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
.set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

Design specific constrain

Not needed.
Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects

Application

FSBL
Xilinx default FSBL

Hello TE0808
Hello TE0808 is a Xilinx Hello World example as endless loop instead of one console output.
Additional Software

No additional software is needed.
Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to “Change History” of this page and select older document revision number.

<table>
<thead>
<tr>
<th>Date</th>
<th>Document Revision</th>
<th>Authors</th>
<th>Description</th>
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<tr>
<td>2018-07-11</td>
<td>v.21</td>
<td>John Hartfiel</td>
<td>• Design Update</td>
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<td>• typo correction on documentation</td>
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<tr>
<td>2017-11-22</td>
<td>v.10</td>
<td>John Hartfiel</td>
<td>• Update assembly versions with new Flash size</td>
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<td>• Update HW Table Name</td>
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<td>• Update Design</td>
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<td>2017-11-14</td>
<td>v.6</td>
<td>John Hartfiel</td>
<td>• Release 2017.2</td>
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2018-09-18