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Online version of this manual and other related documents can be found at https://wiki.trenz-electronic.de/display/PD/Trenz+Electronic+Documentation
Overview

Linux with basic periphery of TE0808 Starterkit (TEBF0808 Carrier).

Key Features

- TEBF0808
- Linux
- USB
- ETH
- PCIe
- SATA
- SD
- I2C
- RGPIO
- user LED access
- Modified FSBL for Si5345 programming
- Special FSBL for QSPI Programming

Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Vivado</th>
<th>Project Built</th>
<th>Authors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td>TE0808-StarterKit-vivado_2017.4-build_10_20180524091208.zip</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2018-03-29</td>
<td>2017.4</td>
<td>TE0808-StarterKit_noprebuild-vivado_2017.4-build_07_20180329145308.zip</td>
<td>John Hartfiel</td>
<td>new assembly variant</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0808-StarterKit-vivado_2017.4-build_07_20180329145246.zip</td>
<td></td>
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<tr>
<td>2018-02-06</td>
<td>2017.4</td>
<td>TE0808-StarterKit_noprebuild-vivado_2017.4-build_05_20180206082740.zip</td>
<td>John Hartfiel</td>
<td>same clk for both VIO</td>
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<tr>
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<td>TE0808-StarterKit-vivado_2017.4-build_05_20180206082722.zip</td>
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<td>2018-02-05</td>
<td>2017.4</td>
<td>TE0808-StarterKit_noprebuild-vivado_2017.4-build_05_20180205083232.zip</td>
<td>John Hartfiel</td>
<td>solved JTAG/Linux problem</td>
</tr>
<tr>
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<td>TE0808-StarterKit-vivado_2017.4-build_05_20180205083208.zip</td>
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<tr>
<td>2018-01-17</td>
<td>2017.4</td>
<td>TE0808-StarterKit-vivado_2017.4-build_05_20180117094213.zip</td>
<td>John Hartfiel</td>
<td>solved USB problem</td>
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<tr>
<td></td>
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<td>TE0808-StarterKit_noprebuild-vivado_2017.4-build_05_20180117094231.zip</td>
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<td>small board part update</td>
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<tr>
<td>2018-01-15</td>
<td>2017.4</td>
<td>TE0808-StarterKit-vivado_2017.4-build_03_20180115092306.zip</td>
<td>John Hartfiel</td>
<td>rework board part files</td>
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<td>TE0808-StarterKit_noprebuild-vivado_2017.4-build_03_20180115092511.zip</td>
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<td>rework design</td>
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<td>2017-12-18</td>
<td>2017.2</td>
<td>TE0808-StarterKit_noprebuild-vivado_2017.2-build_07_20171219151749.zip</td>
<td>John Hartfiel</td>
<td>initial release</td>
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<td>TE0808-StarterKit-vivado_2017.2-build_07_20171219151728.zip</td>
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Release Notes and Know Issues

<table>
<thead>
<tr>
<th>Issues</th>
<th>Description</th>
<th>Workaround/Solution</th>
<th>To be fixed version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash access on Linux</td>
<td>Device tree is not correct on Linux</td>
<td>add compatibility to &quot;compatible &quot;jedec, spi-nor&quot;&quot;</td>
<td>Solved with 20180524 update</td>
</tr>
<tr>
<td>USB UART Terminal is blocked / SDK Debugging is blocked</td>
<td>This happens only with 2017.4 Linux, when JTAG connection is established on Vivado HW Manager.</td>
<td>Do not use HW Manager connection, or if debugging is nessecary: 1. Boot linux with usb terminal 2. From the terminal: root root mount /dev/eth0 3. Open two new SSH terminals via ethernet: root root , run user application ... 4. Exit and close the usb terminal</td>
<td>Solved with 20180205 update</td>
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</table>

Requirements

Software

<table>
<thead>
<tr>
<th>Software</th>
<th>Version</th>
<th>Note</th>
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<tbody>
<tr>
<td>Vivado</td>
<td>2017.4</td>
<td>needed</td>
</tr>
<tr>
<td>SDK</td>
<td>2017.4</td>
<td>needed</td>
</tr>
<tr>
<td>PetaLinux</td>
<td>2017.4</td>
<td>needed</td>
</tr>
</tbody>
</table>

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

<table>
<thead>
<tr>
<th>Module Model</th>
<th>Board Part Short Name</th>
<th>PCB Revision Support</th>
<th>DDR</th>
<th>QSPI Flash</th>
<th>Others</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0808-ES1</td>
<td>es1_sk</td>
<td>REV02, REV03</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
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<tr>
<td>TE0808-ES2</td>
<td>es2_sk</td>
<td>REV03, REV04</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-2ES2</td>
<td>2es2_sk</td>
<td>REV03, REV04</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-1EA</td>
<td>9eg_1ea_sk</td>
<td>REV04</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-1EB</td>
<td>9eg_1eb_sk</td>
<td>REV04</td>
<td>4GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-1ED</td>
<td>9eg_1eb_sk</td>
<td>REV04</td>
<td>4GB</td>
<td>64MB, 1,0 mm connector</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-1EE</td>
<td>9eg_1eb_sk</td>
<td>REV04</td>
<td>4GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-1EL</td>
<td>9eg_1eb_sk</td>
<td>REV04</td>
<td>4GB</td>
<td>128MB, 1,0 mm connector</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Module Model</td>
<td>Board Part Short Name</td>
<td>PCB Revision Support</td>
<td>DDR</td>
<td>QSPI Flash</td>
<td>Others</td>
<td>Notes</td>
</tr>
<tr>
<td>---------------------------</td>
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<td>----------------------</td>
<td>-----</td>
<td>------------</td>
<td>--------</td>
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<tr>
<td>TE0808-04-09EG-2IB</td>
<td>9eg_2ib_sk</td>
<td>REV04</td>
<td>4GB</td>
<td>64MB</td>
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<td></td>
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<tr>
<td>TE0808-04-09EG-2IE</td>
<td>9eg_2ib_sk</td>
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<td>TE0808-04-06EG-1E3</td>
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<td>REV04</td>
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<td>128MB</td>
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<td>1,0 mm connector</td>
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<tr>
<td>TE0808-04-15EG-1EB</td>
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<td>4GB</td>
<td>64MB</td>
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<td></td>
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<tr>
<td>TE0808-04-15EG-1EE</td>
<td>15eg_1eb_sk</td>
<td>REV04</td>
<td>4GB</td>
<td>128MB</td>
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</table>

Note: Design contains also Board Part Files for TE0808 only configuration, this boart part files are not used for this reference design.

Design supports following carriers:

<table>
<thead>
<tr>
<th>Carrier Model</th>
<th>Notes</th>
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<td>TEBF0808</td>
<td>Used as reference carrier.</td>
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Additional HW Requirements:

<table>
<thead>
<tr>
<th>Additional Hardware</th>
<th>Notes</th>
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Content

For general structure and of the reference design, see Project Delivery

Design Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
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</thead>
<tbody>
<tr>
<td>Vivado</td>
<td>&lt;design name&gt;/block_design&lt;br&gt;&lt;design name&gt;/constraints&lt;br&gt;&lt;design name&gt;/ip_lib</td>
<td>Vivado Project will be generated by TE Scripts</td>
</tr>
<tr>
<td>SDK/HSI</td>
<td>&lt;design name&gt;/sw_lib</td>
<td>Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI</td>
</tr>
<tr>
<td>PetaLinux</td>
<td>&lt;design name&gt;/os/petalinux</td>
<td>PetaLinux template with current configuration</td>
</tr>
</tbody>
</table>

Additional Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIS345</td>
<td>&lt;design name&gt;/misc/SIS345</td>
<td>SIS345 Project with current PLL Configuration</td>
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</tbody>
</table>

Prebuilt

<table>
<thead>
<tr>
<th>File</th>
<th>File-Extension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIF-File</td>
<td>*.bif</td>
<td>File with description to generate Bin-File</td>
</tr>
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### File

<table>
<thead>
<tr>
<th>File</th>
<th>File-Extension</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>BIN-File</td>
<td>*.bin</td>
<td>Flash Configuration File with Boot-Image (Zynq-FPGAs)</td>
</tr>
<tr>
<td>BIT-File</td>
<td>*.bit</td>
<td>FPGA (PL Part) Configuration File</td>
</tr>
<tr>
<td>DebugProbes-File</td>
<td>*.ltx</td>
<td>Definition File for Vivado/Vivado Labtools Debugging Interface</td>
</tr>
<tr>
<td>Diverse Reports</td>
<td>---</td>
<td>Report files in different formats</td>
</tr>
<tr>
<td>Hardware-Platform-Specification-Files</td>
<td>*.hdf</td>
<td>Exported Vivado Hardware Specification for SDK/HSI and PetaLinux</td>
</tr>
<tr>
<td>LabTools Project-File</td>
<td>*.lpr</td>
<td>Vivado Labtools Project File</td>
</tr>
<tr>
<td>OS-Image</td>
<td>*.ub</td>
<td>Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)</td>
</tr>
<tr>
<td>Software-Application-File</td>
<td>*.elf</td>
<td>Software Application for Zynq or MicroBlaze Processor Systems</td>
</tr>
</tbody>
</table>

### Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0808 "StarterKit" Reference Design
Design Flow

⚠️ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- Vivado/SDK/SDSoC#XilinxSoftware-BasicUserGuides
- Vivado Projects
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with ".\_create_win_setup.cmd" on Windows OS and "\_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. \_create_win_setup.cmd/\_create_linux_setup.sh and follow instructions on shell:

2. Press 0 and enter for minimum setup

3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)

4. Create Project
   a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado\_create\_project\_guimode.cmd"
   Note: Select correct one, see TE Board Part Files
   Important: Use Board Part Files, which ends with \*\_tebf0808
5. Create HDF and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
      Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder

6. Create Linux (bl31.elf, uboot.elf and image.ub) with exported HDF
   a. HDF is exported to "prebuilt\hardware\<short name>"
      Note: HW Export from Vivado GUI create another path as default workspace.
   b. Create Linux images on VM, see PetaLinux KICKstart
      i. Use TE Template from /os/petalinux
         Note: run init_config.sh before you start petalinux config. This will set correct temporary path variable.

7. Add Linux files (bl31.elf, uboot.elf and image.ub) to prebuilt folder
   a. "prebuilt\os\petalinux\default" or "prebuilt\os\petalinux\<short name>"
      Notes: Scripts select "prebuilt\os\petalinux\<short name>", if exist, otherwise "prebuilt\os\petalinux\default"

8. Generate Programming Files with HSI/SDK
   a. Run on Vivado TCL: TE::sw_run_hsi
      Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
   b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk
      Note: See SDK Projects
Launch

Programming

⚠️ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp u-boot
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup
4. Copy image.ub on SD-Card
5. Insert SD-Card

SD

1. Copy image.ub and Boot.bin on SD-Card.
   • For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Set Boot Mode to SD-Boot.
3. Insert SD-Card in SD-Slot.

JTAG

Not used on this Example.

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (JTAG XMOD)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)
   Note: See TRM of the Carrier, which is used.
4. (Optional) Insert PCIe Card (detection depends on Linux driver. Only some basic drivers are installed)
5. (Optional) Connect Sata Disc
7. (Optional) Connect Network Cable
8. Power On PCB
   Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from SD into OCM, 2. FSBL loads ATF (bl31.elf) and U-boot from SD/QSPI into DDR, 3. U-boot load Linux from SD into DDR.

Linux

1. Open Serial Console (e.g. putty)
   a. Speed: 115200
   b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is "USB1")
2. Linux Console:
   Note: Wait until Linux boot finished For Linux Login use:
   a. User Name: root
   b. Password: root
3. You can use Linux shell now.
   a. I2C 0 Bus type: i2cdetect -y -r 0
   b. ETH0 works with udhcpc
   c. USB type "lsusb" or connect USB device
   d. PCIe type "lspci"

Vivado Hardware Manager

Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).

- RGPIO Interface:
  - Set Bit 31-28 to "1010" to activat RGPIO Interface of Master or Slave CPLD.
    - Description: TEBF0808 Master CPLD#RGPIO, TEBF0808 Slave CPLD#RGPIO
- LED Control:
  - XMOD 2(without green dot) and HD LED are accessible.
System Design - Vivado

Block Design

PS Interfaces

Activated interfaces:

<table>
<thead>
<tr>
<th>Type</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR</td>
<td></td>
</tr>
<tr>
<td>QSPI</td>
<td>MIO</td>
</tr>
<tr>
<td>SD0</td>
<td>MIO</td>
</tr>
<tr>
<td>SD1</td>
<td>MIO</td>
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<td>CAN0</td>
<td>EMIO</td>
</tr>
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<td>I2C0</td>
<td>MIO</td>
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<td>PJTAG0</td>
<td>MIO</td>
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<td>UART0</td>
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<td>GPIO0</td>
<td>MIO</td>
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<td>TTC0..3</td>
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</tr>
<tr>
<td>GEM3</td>
<td>MIO</td>
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</table>
### Constrains

#### Basic module constrains

```plaintext
_i_bitgen.xdc
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

#### Design specific constrain

```plaintext
_i_io.xdc

# LED HD SCD J3:31
set_property PACKAGE_PIN J14 [get_ports {LED_HD[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {LED_HD[0]}]

# LED XMOD SC17 J3:48
set_property PACKAGE_PIN B13 [get_ports {LED_XMOD2[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {LED_XMOD2[0]}]

# System Controller IP
set_property PACKAGE_PIN A15 [get_ports BASE_sc10_io]
set_property PACKAGE_PIN B15 [get_ports BASE_sc11]
set_property PACKAGE_PIN C13 [get_ports BASE_sc12]
set_property PACKAGE_PIN C14 [get_ports BASE_sc13]
set_property PACKAGE_PIN E13 [get_ports BASE_sc14]
set_property PACKAGE_PIN E14 [get_ports BASE_sc15]
set_property PACKAGE_PIN G13 [get_ports BASE_sc5]
set_property PACKAGE_PIN J15 [get_ports BASE_sc6]
set_property PACKAGE_PIN K15 [get_ports BASE_sc7]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc5]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc6]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc7]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc10_io]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc11]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc12]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc13]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc14]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc15]

# PLL
#set_property PACKAGE_PIN AH6 [get_ports {si570_clk_p[0]}]
#set_property IOSTANDARD LVDS [get_ports {si570_clk_p[0]}]
#set_property IOSTANDARD LVDS [get_ports {si570_clk_n[0]}]
# Clocks
#set_property PACKAGE_PIN J8 [get_ports {B229_CLK1_clk_p[0]}]
```
#set_property PACKAGE_PIN F25 [get_ports {B128_CLK0_clk_p[0]}]
# SFP
#set_property PACKAGE_PIN G8 [get_ports {B230_CLK0_clk_p}]
# B230_RX3_P
#set_property PACKAGE_PIN A4 [get_ports {SFP1_rxp}]
# B230_TX3_P
#set_property PACKAGE_PIN A8 [get_ports {SFP1_txp}]
# B230_RX2_P
#set_property PACKAGE_PIN B2 [get_ports {SFP2_rxp}]
# B230_TX2_P
#set_property PACKAGE_PIN B6 [get_ports {SFP2_txp}]

# Audio Codec
# LRCLK   J3:49 B47_L9_N
# BCLK    J3:51 B47_L9_P
# DAC_SDATA   J3:53 B47_L7_N
# ADC_SDATA   J3:55 B47_L7_P
set_property PACKAGE_PIN G14 [get_ports LRCLK ]
set_property PACKAGE_PIN G15 [get_ports BCLK ]
set_property PACKAGE_PIN E15 [get_ports DAC_SDATA ]
set_property PACKAGE_PIN F15 [get_ports ADC_SDATA ]
set_property IOSTANDARD LVCMOS18 [get_ports LRCLK ]
set_property IOSTANDARD LVCMOS18 [get_ports BCLK ]
set_property IOSTANDARD LVCMOS18 [get_ports DAC_SDATA ]
set_property IOSTANDARD LVCMOS18 [get_ports ADC_SDATA ]

# CAN
# CAN RX SC19 J3:52 B47_L2_P
# CAN TX SC18 J3:50 B47_L2_N
# CAN S SC16 J3:46 B47_L3_N
set_property PACKAGE_PIN A13 [get_ports CAN_0_S ]
set_property IOSTANDARD LVCMOS18 [get_ports CAN_0_S ]
set_property PACKAGE_PIN B14 [get_ports CAN_0_rx ]
set_property IOSTANDARD LVCMOS18 [get_ports CAN_0_rx ]
set_property PACKAGE_PIN A14 [get_ports CAN_0_tx ]
set_property IOSTANDARD LVCMOS18 [get_ports CAN_0_tx ]
Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects

Application

FSBL

TE modified 2017.4 FSBL

Changes:

- Si5345Configuration, PCIe Reset over GPIO see xfsbl_board.c and xfsbl_board.h
- Add Si5345-Registers.h, si5345.c, si5345.h

zynqmp_fsbl_flash

TE modified 2017.4 FSBL

Changes:

- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation

PMU

Xilinx default PMU firmware.

Hello TE0808

Hello TE0808 is a Xilinx Hello World example as endless loop instead of one console output.

U-Boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.
Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

Config

No changes.

U-Boot

- Change platform-top.h

```c
#include <configs/platform-auto.h>
define CONFIG_SYS_BOOTM_LEN 0xF000000

define DFU_ALT_INFO_RAM \
   "dfu_ram_info=" \  
   "setenv dfu_alt_info " \  
   "image.ub ram $netstart 0x1e000000\0" \  
   "dfu_ram=run dfu_ram_info && dfu 0 ram 0\0" \  
   "thor_ram=run dfu_ram_info && thordown 0 ram 0\0"

define DFU_ALT_INFO \  
   DFU_ALT_INFO_RAM

/*Required for uartless designs */
ifndef CONFIG_BAUDRATE
define CONFIG_BAUDRATE 115200
ifdef CONFIG_DEBUG_UART
ifndef CONFIG_DEBUG_UART
endif
endif

/*select sd instead of mmc for autoboot */
define CONFIG_BOOTCOMMAND "run uenvboot; mmcinfo && fatload mmc 1 ${netstart} ${kernel_img};bootm ${netstart}""
&sdhci1 {
    // disable-wp;
    no-1-8-v;
    
};

/* USB */
&dwc3_0 {
    status = "okay";
    dr_mode = "host";
};

/* ETH PHY */
&gem3 {
    phy-handle = <&phy0>;
    phy0: phy0@1 {
        device_type = "ethernet-phy";
        reg = <1>;
    };
};

/* QSPI */
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash0@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};

/* I2C */
&i2c0 {
    i2cswitch@73 { // u
        compatible = "nxp,pca9548";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x73>;
        i2c-mux-idle-disconnect;

        i2c@2 { // PCIe
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <2>;
        };
        i2c@3 { // i2c SFP
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <3>;
        };
    };
}
i2c@4 { // i2c SFP
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <4>;
};

i2c@5 { // i2c EEPROM
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <5>;
};

i2c@6 { // i2c FMC
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <6>;
    si570_2: clock-generator305d {
        #clock-cells = <0>;
        compatible = "silabs,si570";
        reg = <0x5d>;
        temperature-stability = <50>;
        factory-fout = <156250000>;
        clock-frequency = <78800000>;
    };
};

i2c@7 { // i2c USB HUB
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <7>;
};

i2cswitch@77 { // u
    compatible = "nxp, pca9548";
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <0x77>;
    i2c-mux-idle-disconnect;

i2c@0 { // i2c PMOD
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <0>;
};

i2c@1 { // i2c Audio Codec
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <1>;
    adau1761: adau1761@38 {
        compatible = "adi, adau1761";
        reg = <0x38>;
    };
    /*
     adau1761: adau1761@38 {
     compatible = "adi, adau1761";
     reg = <0x38>;
     };
     */
};

i2c@2 { // i2c FireFly A
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <2>;
};

i2c@3 { // i2c FireFly B
#address-cells = <1>;
#size-cells = <0>;
reg = <3>;
);

i2c@4 { // i2c PLL
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <4>;
    }

i2c@5 { // i2c SC
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <5>;
    }

i2c@6 { // i2c
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <6>;
    }

i2c@7 { // i2c
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <7>;
    }
    }
    
/* UNUSED DMA disable */

&lpd_dma_chan1 {
    status = "disabled";
    };

&lpd_dma_chan2 {
    status = "disabled";
    };

&lpd_dma_chan3 {
    status = "disabled";
    };

&lpd_dma_chan4 {
    status = "disabled";
    };

&lpd_dma_chan5 {
    status = "disabled";
    };

&lpd_dma_chan6 {
    status = "disabled";
    };

&lpd_dma_chan7 {
    status = "disabled";
    };

&lpd_dma_chan8 {
    status = "disabled";
    };

Kernel

Deactivate:

- CONFIG_CPU_IDLE (only needed to fix JTAG Debug issue)
- CONFIG_CPU_FREQ (only needed to fix JTAG Debug issue)

Rootfs

Activate:

- i2c-tools

Applications

startup

Script App to load init.sh from SD Card if available.

See: `os\petalinux\project-spec\meta-user\recipes-apps\startup\files`

adau1761init

Audio initialisation.
Additional Software

SI5345

Download ClockBuilder Pro for SI5345

1. Install and start ClockBuilder
2. Open "/misc/SI5345/Si5345-RevB-0808-02A-Project.slabtimeproj"
3. Modify settings
4. Export Register File select C code header save to file
5. Replace Header files from FSBL template with generated file
Appx. A: Change History and Legal Notices

Document Change History

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<td>Solved known issues</td>
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<td>v.18</td>
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