# Table of Contents

1 Table of Contents ........................................................................................................................................... 2
2 Table of Figures ............................................................................................................................................... 4
3 Table of Tables ............................................................................................................................................... 5
4 Overview ....................................................................................................................................................... 7
4.1 Key Features ............................................................................................................................................... 7
4.2 Revision History ...................................................................................................................................... 7
4.3 Release Notes and Know Issues ............................................................................................................... 9
4.4 Requirements .......................................................................................................................................... 9
4.4.1 Software ........................................................................................................................................... 9
4.4.2 Hardware ......................................................................................................................................... 9
4.5 Content .................................................................................................................................................. 11
4.5.1 Design Sources ............................................................................................................................... 11
4.5.2 Additional Sources ........................................................................................................................ 12
4.5.3 Prebuilt ........................................................................................................................................... 12
4.5.4 Download ...................................................................................................................................... 12
5 Design Flow ................................................................................................................................................ 13
6 Launch ......................................................................................................................................................... 15
6.1 Programming .......................................................................................................................................... 15
6.1.1 QSPI ................................................................................................................................................. 15
6.1.2 SD .................................................................................................................................................. 15
6.1.3 JTAG .............................................................................................................................................. 15
6.2 Usage ..................................................................................................................................................... 15
7 System Design - Vivado ............................................................................................................................. 17
7.1 Block Design ......................................................................................................................................... 17
7.1.1 PS Interfaces .................................................................................................................................. 17
7.2 Constrains ............................................................................................................................................. 18
7.2.1 Basic module constrains ............................................................................................................... 18
7.2.2 Design specific constrains ............................................................................................................ 18
8 Software Design - SDK/HSI ......................................................................................................................... 19
8.1 Application ............................................................................................................................................ 19
8.1.1 zynqmp_fsb1 .................................................................................................................................. 19
8.1.2 zynqmp_fsb1_flash ....................................................................................................................... 19
8.1.3 hello_te0808 ................................................................................................................................... 19
9 Additional Software .................................................................................................................................. 20
10 Appx. A: Change History and Legal Notices ............................................................................................ 21
# Table of Figures
3 Table of Tables
Online version of this manual and other related documents can be found at https://wiki.trenz-electronic.de/display/PD/Trenz+Electronic+Documentation
4 Overview

Design Example with minimum PS Setup (DDR, QSPI, UART0) only for custom boards or easier debug via SDK.

4.1 Key Features

- QSPI
- SDK
- Custom Carrier (minimum PS Design with available module components only)
- Special FSBL for QSPI Programming

4.2 Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Vivado</th>
<th>Project Built</th>
<th>Authors</th>
<th>Description</th>
</tr>
</thead>
</table>
| 2018-07-11 | 2018.2 | TE0808-test_board_noprebuilt-vivado_2018.2-build_02_20180711143743.zip    | John Hartfiel | • additional notes for FSBL generated with Win SDK  
• changed *.bif                                             |
|            |        | TE0808-test_board-vivado_2018.2-build_02_20180711143702.zip                |                |                                                                                                           |
| 2018-03-29 | 2017.4 | TE0808-test_board-vivado_2017.4-build_07_20180329151341.zip                | John Hartfiel | • new assembly variant                                                                                   |
|            |        | TE0808-test_board_noprebuilt-vivado_2017.4-build_07_20180329151355.zip    |                |                                                                                                           |
| 2018-01-16 | 2017.4 | TE0808-test_board-vivado_2017.4-build_04_20180116144644.zip                | John Hartfiel | • Update Board Part for TEBF0808  
• no changes for test board design and minimal board parts                                            |
<p>|            |        | TE0808-test_board_noprebuilt-vivado_2017.4-build_04_20180116144657.zip    |                |                                                                                                           |</p>
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<th>Date</th>
<th>Vivado</th>
<th>Project Built</th>
<th>Authors</th>
<th>Description</th>
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<td>2017.4</td>
<td>TE0808-test_board-vivado_2017.4-build_03_20180115084954.zip</td>
<td>John Hartfiel</td>
<td>• rework Board Part Files</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0808-test_board_noprebuilt-vivado_2017.4-build_03_20180115085020.zip</td>
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<td></td>
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<tr>
<td>2017-12-20</td>
<td>2017.2</td>
<td>TE0808-test_board-vivado_2017.2-build_07_2017122192501.zip</td>
<td>John Hartfiel</td>
<td>• Update Board Part Files</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0808-test_board_noprebuilt-vivado_2017.2-build_07_2017122192448.zip</td>
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<td>2017-11-22</td>
<td>2017.2</td>
<td>TE0808-test_board-vivado_2017.2-build_05_20171122080211.zip</td>
<td>John Hartfiel</td>
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<td></td>
<td></td>
<td>TE0808-test_board_noprebuilt-vivado_2017.2-build_05_20171122080228.zip</td>
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<td>• Regenerate design</td>
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<tr>
<td>2017-11-16</td>
<td>2017.2</td>
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<td>John Hartfiel</td>
<td>• Update Board Part CSV File with new Flash</td>
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<tr>
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<td>TE0808-test_board_noprebuilt-vivado_2017.2-build_05_20171116151600.zip</td>
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<td>assembly variants</td>
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### 4.3 Release Notes and Know Issues

<table>
<thead>
<tr>
<th>Issues</th>
<th>Description</th>
<th>Workaround</th>
<th>To be fixed version</th>
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<tbody>
<tr>
<td>No known issues</td>
<td>---</td>
<td>---</td>
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### 4.4 Requirements

#### 4.4.1 Software

<table>
<thead>
<tr>
<th>Software</th>
<th>Version</th>
<th>Note</th>
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<tr>
<td>Vivado</td>
<td>2018.2</td>
<td>needed</td>
</tr>
<tr>
<td>SDK</td>
<td>2018.2</td>
<td>needed</td>
</tr>
</tbody>
</table>

#### 4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.¹  
Complete List is available on <design name>/board_files/*_board_files.csv  
Design supports following modules:

---

¹ [https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files](https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files)
<table>
<thead>
<tr>
<th>Module Model</th>
<th>Board Part Short Name</th>
<th>PCB Revision Support</th>
<th>DDR</th>
<th>QSPI Flash</th>
<th>Others</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0808-ES1</td>
<td>es1</td>
<td>REV02, REV03</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Xilinx has stopped ES1 support with 2018.2, please use 2017.4 reference design</td>
</tr>
<tr>
<td>TE0808-ES2</td>
<td>es2</td>
<td>REV03, REV04</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-2ES2</td>
<td>2es2</td>
<td>REV03, REV04</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-1EA</td>
<td>9eg_1ea</td>
<td>REV04</td>
<td>2GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-1EB</td>
<td>9eg_1eb</td>
<td>REV04</td>
<td>4GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-1ED</td>
<td>9eg_1eb</td>
<td>REV04</td>
<td>4GB</td>
<td>64MB</td>
<td></td>
<td>1,0 mm connector</td>
</tr>
<tr>
<td>TE0808-04-09EG-1EE</td>
<td>9eg_1eb</td>
<td>REV04</td>
<td>4GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-1EL</td>
<td>9eg_1eb</td>
<td>REV04</td>
<td>4GB</td>
<td>128MB</td>
<td></td>
<td>1,0 mm connector</td>
</tr>
<tr>
<td>TE0808-04-09EG-2IB</td>
<td>9eg_2ib</td>
<td>REV04</td>
<td>4GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-09EG-2IE</td>
<td>9eg_2ib</td>
<td>REV04</td>
<td>4GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-06EG-1EE</td>
<td>6eg_1ee</td>
<td>REV04</td>
<td>4GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-06EG-1E3</td>
<td>6eg_1ee</td>
<td>REV04</td>
<td>4GB</td>
<td>128MB</td>
<td></td>
<td>1,0 mm connector</td>
</tr>
<tr>
<td>Module Model</td>
<td>Board Part Short Name</td>
<td>PCB Revision Support</td>
<td>DDR</td>
<td>QSPI Flash</td>
<td>Others</td>
<td>Notes</td>
</tr>
<tr>
<td>-------------------</td>
<td>-----------------------</td>
<td>----------------------</td>
<td>-----</td>
<td>------------</td>
<td>--------</td>
<td>-------</td>
</tr>
<tr>
<td>TE0808-04-15EG-1EB</td>
<td>15eg_1eb</td>
<td>REV04</td>
<td>4GB</td>
<td>64MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0808-04-15EG-1EE</td>
<td>15eg_1eb</td>
<td>REV04</td>
<td>4GB</td>
<td>128MB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: Design contains also Board Part Files for TE0808+TEBF0808 configuration, this board part files are not used for this reference design.

Design supports following carriers:

<table>
<thead>
<tr>
<th>Carrier Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Custom PCB</td>
<td>use simple Board Part files, if MIO connected is different to TEBF0808</td>
</tr>
<tr>
<td>TEBF0808</td>
<td>Used as reference carrier.</td>
</tr>
<tr>
<td>TEBT0808</td>
<td>Change manually UART0 to UART1 (MIO68...69) and regenerate design</td>
</tr>
</tbody>
</table>

Additional HW Requirements:

<table>
<thead>
<tr>
<th>Additional Hardware</th>
<th>Notes</th>
</tr>
</thead>
</table>

### 4.5 Content

For general structure and of the reference design, see [Project Delivery](https://wiki.trenz-electronic.de/display/PD/Project+Delivery)

### 4.5.1 Design Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vivado</td>
<td>&lt;design name&gt;/block_design &lt;design name&gt;/constraints &lt;design name&gt;/ip_lib</td>
<td>Vivado Project will be generated by TE Scripts</td>
</tr>
<tr>
<td>SDK/HSI</td>
<td>&lt;design name&gt;/sw_lib</td>
<td>Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI</td>
</tr>
</tbody>
</table>

---

2 https://wiki.trenz-electronic.de/display/PD/Project+Delivery
4.5.2 Additional Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
</table>

4.5.3 Prebuilt

<table>
<thead>
<tr>
<th>File</th>
<th>File-Extension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIF-File</td>
<td>*.bif</td>
<td>File with description to generate Bin-File</td>
</tr>
<tr>
<td>BIN-File</td>
<td>*.bin</td>
<td>Flash Configuration File with Boot-Image (Zynq-FPGAs)</td>
</tr>
<tr>
<td>BIT-File</td>
<td>*.bit</td>
<td>FPGA (PL Part) Configuration File</td>
</tr>
<tr>
<td>Diverse Reports</td>
<td>___</td>
<td>Report files in different formats</td>
</tr>
<tr>
<td>Hardware-Platform-</td>
<td>*.hdf</td>
<td>Exported Vivado Hardware Specification for SDK/HSI and PetaLinux</td>
</tr>
<tr>
<td>Specification-Files</td>
<td>___</td>
<td></td>
</tr>
<tr>
<td>LabTools Project-File</td>
<td>*.lpr</td>
<td>Vivado Labtools Project File</td>
</tr>
<tr>
<td>Software-Application-File</td>
<td>*.elf</td>
<td>Software Application for Zynq or MicroBlaze Processor Systems</td>
</tr>
</tbody>
</table>

4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0808 "Test Board" Reference Design³

5 Design Flow

Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- Vivado/SDK/SDSoC
- Vivado Projects
- Project Delivery

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example: \<design name>)
4. Create Project
   a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
   b. Note: Select correct one, see TE Board Part Files
   * Important: Use Board Part Files, which did not ends with * _tebf0808
5. Create HDF and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
   b. Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Generate Programming Files with HSI/SDK

---

5 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects
6 https://wiki.trenz-electronic.de/display/PD/Project+Delivery
7 https://wiki.trenz-electronic.de/display/PD/Project+Delivery#ProjectDelivery-Currentlylimitationsoffunctionality
8 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files
a. Run on Vivado TCL: TE::sw_run_hsi
   Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk
   Note: See SDK Projects\(^9\)

\(^9\) https://wiki.trenz-electronic.de/display/PD/SDK+Projects
6 Launch

6.1 Programming

⚠️ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

6.1.1 QSPI

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp hello_te0808
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup

Use SDK instead of Vivado is also possible, see: SDK Projects#Xilinx%22HelloWorld%22onZynqMP

6.1.2 SD

This does not work, because SD controller is not selected on PS.

6.1.3 JTAG

Load configuration and Application with SDK Debugger into device, see:
- SDK Projects
- SDK Projects

6.2 Usage

QSPI Boot:
1. Prepare HW like described on section Programming (see page 15)
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI Card as Boot Mode
   Note: See TRM of the Carrier, which is used.
4. Power On PCB
   Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from QSPI into OCM, 2. FSBL loads application into DDR

Debugging:

---

10 https://wiki.trenz-electronic.de/pages/viewpage.action?pageId=14746264#Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging
12 https://wiki.trenz-electronic.de/display/PD/SDK+Projects
13 https://wiki.trenz-electronic.de/display/PD/SDK+Projects#SDKProjects-DebugSoftwareApplication
• SDK Projects\(^{14}\)
• SDK Projects\(^{15}\)

\(^{14}\) https://wiki.trenz-electronic.de/display/PD/SDK+Projects
\(^{15}\) https://wiki.trenz-electronic.de/display/PD/SDK+Projects#SDKProjects-DebugSoftwareApplication
7 System Design - Vivado

7.1 Block Design

7.1.1 PS Interfaces

Activated interfaces:

<table>
<thead>
<tr>
<th>Type</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR</td>
<td></td>
</tr>
<tr>
<td>QSPI</td>
<td>MIO</td>
</tr>
<tr>
<td>UART0</td>
<td>MIO, please select other one, if you have connected uart to second controller or other MIO</td>
</tr>
<tr>
<td>SWDT0..1</td>
<td></td>
</tr>
<tr>
<td>TTC0..3</td>
<td></td>
</tr>
</tbody>
</table>
7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen.xdc

set_property BITSTREAMGENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAMCONFIG.UNUSEDPIN PULLNONE [current_design]

7.2.2 Design specific constrain

Not needed.
8 Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects\textsuperscript{16}

8.1 Application

8.1.1 zynqmp_fsbl

Xilinx default FSBL

8.1.2 zynqmp_fsbl_flash

TE modified 2018.2 FSBL

Changes:

- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation

8.1.3 hello_te0808

Hello TE0808 is a Xilinx Hello World example as endless loop instead of one console output.

---

\textsuperscript{16} https://wiki.trenz-electronic.de/display/PD/SDK+Projects
9 Additional Software

No additional software is needed.
10 Appx. A: Change History and Legal Notices

10.1 Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

<table>
<thead>
<tr>
<th>Date</th>
<th>Document Revision</th>
<th>Authors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018-07-11</td>
<td>v.21(see page 6)</td>
<td>John Hartfiel 17</td>
<td>• Release 2018.2</td>
</tr>
<tr>
<td>29.03.2018</td>
<td>v.20</td>
<td>John Hartfiel 18</td>
<td>• new assembly variant</td>
</tr>
<tr>
<td>2018-02-08</td>
<td>v.19</td>
<td>John Hartfiel 19</td>
<td>• Release 2017.4</td>
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<tr>
<td>2017-12-20</td>
<td>v.14</td>
<td>John Hartfiel 20</td>
<td>• Design Update</td>
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<td></td>
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<td></td>
<td>• typo correction on documentation</td>
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<tr>
<td>2017-11-22</td>
<td>v.10</td>
<td>John Hartfiel 21</td>
<td>• Update assembly versions with new Flash size</td>
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<td>• Update HW Table Name</td>
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<td>v.6</td>
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<td>John Hartfiel 23</td>
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</tr>
</tbody>
</table>

10.2 Legal Notices

10.3 Data privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

17 https://wiki.trenz-electronic.de/display/-j.hartfiel
18 https://wiki.trenz-electronic.de/display/-j.hartfiel
19 https://wiki.trenz-electronic.de/display/-j.hartfiel
20 https://wiki.trenz-electronic.de/display/-j.hartfiel
21 https://wiki.trenz-electronic.de/display/-j.hartfiel
22 https://wiki.trenz-electronic.de/display/-j.hartfiel
23 https://wiki.trenz-electronic.de/display/-j.hartfiel
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10.8 Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

10.9 REACH, RoHS and WEEE

**REACH**

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of **REACH**\(^24\). The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no **SVHC (Substances of Very High Concern)** on the

\(^{24}\)http://guidance.echa.europa.eu/
Candidate List\textsuperscript{25} are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0.1 \% weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA)\textsuperscript{26}.

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE


Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

\textsuperscript{25} https://echa.europa.eu/candidate-list-table
\textsuperscript{26} http://www.echa.europa.eu/