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Online version of this manual and other related documents can be found at https://wiki.trenz-electronic.de/display/PD/Trenz+Electronic+Documentation
Overview

Zynq PS Design with DDR Less FSBL Example.

Key Features

- UART
- QSPI
- Modified FSBL for DDR Less Zynq
- Special FSBL for QSPI programming

Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Vivado</th>
<th>Project Built</th>
<th>Authors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018-08-14</td>
<td>2018.2</td>
<td>TE0722-test_board-vivado_2018.2-build_02_20180815123557.zip</td>
<td>John Hartfiel</td>
<td>initial release</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TE0722-test_board_noprebuild-vivado_2018.2-build_02_20180815123610.zip</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Release Notes and Know Issues

<table>
<thead>
<tr>
<th>Issues</th>
<th>Description</th>
<th>Workaround</th>
<th>To be fixed version</th>
</tr>
</thead>
<tbody>
<tr>
<td>No known issues</td>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
</tbody>
</table>

Requirements

Software

<table>
<thead>
<tr>
<th>Software</th>
<th>Version</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vivado</td>
<td>2018.2</td>
<td>needed</td>
</tr>
<tr>
<td>SDK</td>
<td>2018.2</td>
<td>needed</td>
</tr>
</tbody>
</table>

Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](http://www.trenz-electronic.de).

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

<table>
<thead>
<tr>
<th>Module Model</th>
<th>Board Part Short Name</th>
<th>PCB Revision Support</th>
<th>DDR</th>
<th>QSPI Flash</th>
<th>Others</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0722-02</td>
<td>10</td>
<td>REV02, REV01</td>
<td>--</td>
<td>16MB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TE0722-02-I</td>
<td>10_i</td>
<td>REV02, REV01</td>
<td>--</td>
<td>16MB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Design supports following carriers:

<table>
<thead>
<tr>
<th>Carrier Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Additional HW Requirements:

<table>
<thead>
<tr>
<th>Additional Hardware</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE0790</td>
<td>for JTAG, UART</td>
</tr>
<tr>
<td></td>
<td>external 3.3V power supply</td>
</tr>
</tbody>
</table>

Content

For general structure and of the reference design, see Project Delivery

Design Sources

<table>
<thead>
<tr>
<th>Type</th>
<th>Location</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vivado</td>
<td>&lt;design name&gt;/block_design</td>
<td>Vivado Project will be generated by TE Scripts</td>
</tr>
<tr>
<td></td>
<td>&lt;design name&gt;/constraints</td>
<td></td>
</tr>
<tr>
<td></td>
<td>&lt;design name&gt;/ip_lib</td>
<td></td>
</tr>
<tr>
<td>SDK/HSI</td>
<td>&lt;design name&gt;/sw_lib</td>
<td>Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI</td>
</tr>
</tbody>
</table>

Additional Sources

Prebuilt

<table>
<thead>
<tr>
<th>File</th>
<th>File-Extension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIF-File</td>
<td>*.bif</td>
<td>File with description to generate Bin-File</td>
</tr>
<tr>
<td>BIN-File</td>
<td>*.bin</td>
<td>Flash Configuration File with Boot-Image (Zynq-FPGAs)</td>
</tr>
<tr>
<td>BIT-File</td>
<td>*.bit</td>
<td>FPGA (PL Part) Configuration File</td>
</tr>
<tr>
<td>Diverse Reports</td>
<td>---</td>
<td>Report files in different formats</td>
</tr>
<tr>
<td>Hardware-Platform-Specification-Files</td>
<td>*.hdf</td>
<td>Exported Vivado Hardware Specification for SDK/HSI and PetaLinux</td>
</tr>
<tr>
<td>LabTools Project-File</td>
<td>*.lpr</td>
<td>Vivado Labtools Project File</td>
</tr>
<tr>
<td>Software-Application-File</td>
<td>*.elf</td>
<td>Software Application for Zynq or MicroBlaze Processor Systems</td>
</tr>
</tbody>
</table>
Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0722 "Test Board" Reference Design
Design Flow

⚠️ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- Vivado/SDK/SDSoC/XilinxSoftware-BasicUserGuides
- Vivado Projects
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with ";create_win_setup.cmd" on Windows OS and ";create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. ;create_win_setup.cmd;/create_linux_setup.sh and follow instructions on shell:

2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\design name\)
4. Create Project  
   a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"  
      Note: Select correct one, see TE Board Part Files  
5. Create HDF and export to prebuilt folder  
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt  
      Note: Script generate design and export files into 'prebuilt\hardware\<short dir>'. Use GUI is the same, except file export to prebuilt folder  
6. Generate Programming Files with HSI/SDK  
   a. Run on Vivado TCL: TE::sw_run_hsi  
      Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"  
   b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk  
      Note: See SDK Projects

⚠️ TE0722 is without DDR, so special FSBL (sources on reference designs) is needed,  
see also: DDR less ZYNQ Design
Launch

Basic Information, see TE0722 Getting Started

Programming

⚠️ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_openExisting_project_gui_mode.cmd" or if not created, create with "vivado_create_project_gui_mode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp fsbl_app
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup

SD

Xilinx Zynq devices in CLG225 package do not support SD Card boot directly from ROM bootloader. Use QSPI for primary boot and SD for secondary boot only

JTAG

Not used on this Example.

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Power On PCB
   Note: 1. Zynq Boot ROM loads FSBL from QSPI into OCM, 2. FSBL loads bitfile from qsi, 3. FSBL starts application

Baremetal App

Note: UART over J2 is used, this is only available, if PL part is configured.
1. Open Serial Console (e.g. putty)
   a. Speed: 115200
   b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Output:
   a. Default output appears only one time. Reboot device: force ResN Pin to GND for short time, location see: TE0722 Getting Started

   ![Serial Console Output](image1)

   b. alternately Hello TE0722 loop (for 100sec): uncomment loop in fsbl example (fsbl_hooks.c) and regenerate FSBL and Boot.bin

   ![Serial Console Output](image2)
System Design - Vivado

Block Design

PS Interfaces

<table>
<thead>
<tr>
<th>Type</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR</td>
<td>Disabled!</td>
</tr>
<tr>
<td>QSPI</td>
<td>MIO</td>
</tr>
<tr>
<td>SD</td>
<td>MIO</td>
</tr>
<tr>
<td>UART0</td>
<td>EMIO</td>
</tr>
<tr>
<td>I2C1</td>
<td>MIO</td>
</tr>
<tr>
<td>GPIO</td>
<td>MIO</td>
</tr>
<tr>
<td>SWDT0</td>
<td>EMIO</td>
</tr>
<tr>
<td>TTC0..1</td>
<td>EMIO</td>
</tr>
</tbody>
</table>
Constrains

Basic module constrains

<!--_i_bitgen_common.xdc-->

# Common BITGEN related settings for TE0722
#
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]

set_property BITSTREAM.CONFIG.UNUSEDPIN PULLUP [current_design]

Design specific constrain

<!--_iuart_j2xmod.xdc-->

set_property PACKAGE_PIN K15 [get_ports UART_0_txd]
set_property PACKAGE_PIN L13 [get_ports UART_0_rxd]
set_property IOSTANDARD LVCMOS33 [get_ports UART_0_*]
Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects

Application

Source location: `\sw_lib\sw_apps`

**zynqmp_fsbl**

TE modified 2018.2 FSBL

Changes:

- Disable Memory initialisation on main.c
- Add additional console output to fsbl_hooks.c

**zynqmp_fsbl_flash**

TE modified 2018.2 FSBL

Changes:

- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation
Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to “Change History” of this page and select older document revision number.

<table>
<thead>
<tr>
<th>Date</th>
<th>Document Revision</th>
<th>Authors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2019-05-14</td>
<td>v.6</td>
<td>John Hartfiel</td>
<td>• 2018.2 release</td>
</tr>
<tr>
<td>2018-10-14</td>
<td>v.1</td>
<td>John Hartfiel</td>
<td>• Initial release</td>
</tr>
<tr>
<td>All</td>
<td></td>
<td>John Hartfiel</td>
<td></td>
</tr>
</tbody>
</table>

Legal Notices

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Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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2018-09-18