Rev. 03:

1. PCB: changed position of connectors J1-J4. J1, J3: \( \Delta Y -0.8 \text{mm} \); J2, J4: \( \Delta Y -0.9 \text{mm} \)
2. U12 HOLD and WP inputs connected to 3.3V via 10 k\( \Omega \) pull-up resistor.
3. PCB: jumper J8 (CPLD JTAG, EN) moved between P3 - P4
4. Added series R8 to R087 (Hyper RAM CK input)
5. Added pull-up resistor R9 (Hyper RAM CS input)
6. P1 and P2 are interchanged
7. Added PMOD and pin headers labels
8. Renamed nets
9. U5 HyperFlash replaced by HyperRAM