REV02:

1. 2 CPLDs replaced with LCMXO2-700HC-4FG484C (U27)
2. Single SFP connector removed. MGT lanes B129, TX/RX, 1 connected to FMC F
3. DCDC U45 (power supply of 2xSFP and 1xSFP connectors) removed. 2xSFP powered by U11.
4. HDMI lane B505, TX2 connected to DDI_Tx and lane B505, TX3 to DDI_Tx.
5. Supervisor U69 TPS3106E33 replaced with TPS3106E09
6. U17 (85345), IN_SEL0/1 disconnected from CPLD and connected to GND
7. Added new clock source U57 (SD008AI73-XXS-25.000000E). Connected to CPLD. Not fitted
8. I2C pull-ups R154/R155: changed from 4.7k to 1.5kOhm
9. FAN: R285, R330, R260 changed to 27K (P*SENSE)
10. Added fuse F2 (4A). Fuse F1 (1.85A) “not fitted”
11. C54 (PW_R_IN_12V) deleted
12. Removed clock loop-back OUT9P/N – IN92P/N (U17, 55545)
13. Out7 (P) of U17 (clock source 55545) connected to CPLD U27 Bank 5.
14. Signal SD Card detect SD_CD connected to CPLD. MO45 connected to CPLD
15. Signals FMC*_PG_C2M(M2C) pulled-up to 3V3SB (was FMC*_3V3)
16. CLK_OUT U15 (USB PHY), serial resistor value R13 changed from 33 to 0 Ohm
17. EN5311QI Cout value changed from 22uF to 10uF
18. ROM optimization
19. Added connections from CPLD to FMC A and F (x_LA06_SC - x_LA33_SC)
20. Net EN_VCCINT connected also to DCDC U31 (5V_SYS_PL) and U46 (5V_SYS_PS)
21. Added 2 24B EEPROM (U44/U45)
22. Added power-up sequencing
23. MO46 connected to CPLD
24. Signals EN_SFP was renamed to EN_SFP_SSD. 12V_FMC was renamed to 12V_FMC_AF,
   FMC12V_PG to FMCAF_12V_PG
25. Nets names F_LA02/03/04 was swapped.