TEB0911 - FMC A

Title: TEB0911 - FMC A

Number: TEB0911 ZU9EG1E

Date: 2017-10-16

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Rev. 03

Single FMC Commercial Baseboard Snap
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The diagram shows a circuit with various components and labels. The components include resistors (R), capacitors (C), diodes, and other electronic parts. The diagram includes reference designators (U), pin numbers for each component, and voltages for different sections. There are several sections labeled with numbers and letters, indicating different areas of the circuit. The diagram is detailed with specific connections and labels for each part, providing a clear view of the electronic layout.

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**Note:** The diagram represents a printed circuit board (PCB) layout, showing the placement of electronic components and their interconnections. It is useful for engineers and technicians to understand the physical arrangement of the circuit.
In case using R289 remove R282 and U94
REV02:
1. 2 CPLDs replaced with LCMXO2-7000HC-4FG484C (U27)
2. Single SFP connector removed. MGT lanes B129_TX/RX, 1 connected to FMC F
3. DCDC U45 (power supply of 2xSFP and 1xSFP connectors) removed. 2xSFP powered by U11.
4. HDMI lane B505, TX2 connected to DP1_TX and lane B505, TX3 to DP0_TX.
5. Supervisor U69 TPS3106E33 replaced with TPS3106E09
6. U17 (S5345): IN_SEL0/1 disconnected from CPLD and connected to GND
7. Added new clock source U57 (SDS008AI-73-XXX-25.000000E). Connected to CPLD. Not fitted
8. I2C pull-ups R154/R155: changed from 4.7k to 1.5kOhm
9. FAN: R285, R330, R260 changed to 27K (P*SENSE)
10. Added fuse F2 (4A). Fuse F1 (1.85A) "not fitted"
11. C154 (PWR_IN_24V/GND) deleted
12. Removed clock loop-back OUT9PN - IN2PN (U17, S5345)
13. OUT7 (P) of U17 (clock source S5345) connected to CPLD U27 Bank 5.
14. Signal SD Card detect SD_CD connected to CPLD. MIO45 connected to CPLD
15. Signals FMC*_IN180M2(M2C) pulled-up to 3V/SSB (was FMC*_3V3)
16. CLK_OUT U15 (USB PHY), serial resistor value R13 changed from 33 to 0 Ohm
17. EN5311QE Cout value changed from 22uF to 10uF
18. ROM optimization
19. Added connections from CPLD to FMC A and F (x_LA06, SC - x_LA33, SC)
20. Net EN_VCCINT connected also to DCDC U31 (5V_SYS_PL) and U46 (5V_SYS_PS)
21. Added 2 24F EEPROM (U45A45)
22. Added power-up sequencing
23. MIO6 connected to CPLD
24. Signals EN_SFP was renamed to EN_SFP_SSD. 12V_FMC was renamed to 12V_FMC_AF.
25. Nets names F_LA02/03/04 was swapped.

REV03:
1. Signals C_LA27_P/N swapped: C_LA27_P connected to pin R10 (IO_L11P_T1U_N8_GC_67),
   C_LA27_N connected to R9 (IO_L11N_T1U_N9_GC_67) of U1 (XCZU9EG-1FFVB1156)