RESET pin should be held LOW until both supplies become stable.

Each member of a SuperSpeed differential pair should be no more than 1.25 mm than 1.25 mm.

Active LOW

Power enable and overcurrent LOW

USB 0x60 (or 0x58)
TEB0911 - DDR POWER

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TEB0911 - FMC POWER

A4
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Title: TEB0911 - I2C System

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REV02:
1. 2 CPLDs replaced with LCMXO2-7000HC-4FG484C (U27)
2. Single SFP connector removed. MGT lanes B129, TX/RX, 1 connected to FMC F
3. DCDC U45 (power supply of 2xSFP and 1xSFP connectors) removed. 2xSFP powered by U11.
4. HDMI: lane B50_3 connected to DP1_TX and lane B50_3 to DP0_TX
5. Supervisor U69 TPS3106E33 replaced with TPS3106E09
6. U17 (85345): IN_SEL(0) disconnected from CPLD and connected to GND
7. Added new clock source U57 (SDI008AI-73-KXS-25.000000E). Connected to CPLD. Not fitted
8. 12C pull-ups R154/R155: changed from 4.7k to 1.5kOhm
9. FAN: R235, R236 changed to 27K (P*SENSE)
10. Added fuse F2 (4A). Fuse F1 (1.85A) "not fitted"
11. C54 (PWR_IN_24V/GND) deleted
12. Removed clock loop-back OUT9PN - IN2PN (U17, 55345)
13. OUT7 (P) of U17 (clock source 55345) connected to CPLD U27 Bank 5.
14. Signal SD Card detect SD_CD connected to CPLD. MIO45 connected to CPLD
15. Signals FMC*_PG_C2M(M2C) pulled-up to 3.3VSB (was FMC*_3V3)
16. CLK_OUT U15 (USB PHY), serial resistance value increased from 33 to 0 Ohm
17. EN55311IQC, Out value changed from 22uF to 10uF
18. BOM optimization
19. Added connections from CPLD to FMC A and F (x_LA06_SC - x_LA33_SC)
20. New EN, VCCINT connected also to DCDC U31 (5V_SYS_PL) and U46 (5V_SYS_PS)
21. Added 2 24f EEPROM (U45/43)
22. Added power-up sequencing
23. MIO6 connected to CPLD
24. Signals EN_SFP was renamed to EN_SFP_SSD, 12V_FMC was renamed to 12V_FMC_AF, FMC12V_PG to FMC POV_12V_PG
25. Nets names F_LA02/03/04 was swapped.

REV03:
1. Signals C_LA27_P/N swapped: C_LA27_P connected to pin R10 (IO_L11P_T1U_N8_GC_-67), C_LA27_N connected to R9 (IO_L11N_T1U_N9_GC_-67) of U1 (XCZU9EG-1FFVB1156)

REV03a (17.11.2017):
1. Flash N25Q56A11E1240E changed to N25Q512A11G1240E.

REV04:
1. Added SDIO level translator TXS02612RTWR (U39) and 33Ω series resistors on SDIO lines from FPGA side.
2. Added user button S5 and jumper J5 (connected to U27 pin W17).
3. New FAN switch U76-78/U97-99: BTS4141N
4. 4 New FANs: AF65M512MA. Was added an option to use 5V or 12V (default) power rail.
5. Replaced EOL components:
   - TPS2708LDDCR -> TPS22918DBVT (U96)
   - ESD3V3U4ULCE6327XTSA1 -> AOZ8808DI-03 (U28)

REV04a (30.08.2019):
1. Resistor R65 (USB VBUS) replaced by 1kΩ.