Capacitors suitable for ZU9EG, ZU15EG

Title: TEB0911 - FPGA POWER
A4 Number: TEB0911
ZU15EGE
Rev. 04
Date: 18.09.2018
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Filename: ZU_PWR.SchDoc
USB: 0x60 (or 0x58)
EEPROM: 0x51 (0b1010001x)
RESETN pin should be held LOW until both supplies become stable.

LAYOUT NOTES:
Each member of a High-Speed differential pair should be no more than 1.25 mm
Each member of a SuperSpeed differential pair should be no more than 0.13 mm

RESETN pin should be held LOW until both supplies become stable.
REV02:
1. 2 CPLDs replaced with LCMXO2-700HC-4FG484C (U27)
2. Single SFP connector removed. MGT lanes B129, TX/RX, _1 connected to FMC F
3. DCDC U45 (power supply of 2xSFP and 1xSFP connectors) removed. 2xSFP powered by U11.
4. HDMI lane B505, TX2 connected to D51, TX and lane B505, TX3 to D51, TX
5. Supervisor U59 TPS31060 replaced with TPS3106009
6. U17 (SIS5345): IN_SEL0/1 disconnected from CPLD and connected to GND
7. Added new clock source U57 (SD9008AL-73-XXX-25.000000E). Connected to CPLD. Not fitted
8. 12C pull-ups R154/R155 changed from 4.7k to 1.5kOhm
9. FAN: R285, R330, R260 changed to 27K (PSENSE)
10. Added fuse F2 (4A). Fuse F1 (1.85A) “not fitted”
11. C514 (PWREN, 24V/GND) deleted
12. Removed clock loop-back OUT79PN - IN29IN (U17, SIS5345)
13. OUT7 (P) of U17 (clock source SIS5345) connected to CPLD U27 Bank 5.
14. Signal SD Card detect SD_C0 connected to CPLD. MIO45 connected to CPLD
15. Signals FMC*_PG_C2M(M2C) pulled-up to 3V3SB (was FMC*_3V3)
16. CLK_OUT1 U15 (USB PHY), serial resistor value R13 changed from 33 to 0 Ohm
17. EN553111Q: Cout value changed from 22uf to 10uf
18. ROM optimization
19. Added connections from CPLD to FMC A and F (x.LA06_SC - x.LA33_SC)
20. Net EN_VCCINT connected also to DCDC U31 (5V_SYS_PL) and U46 (5V_SYS_PS)
21. Added 2x4 EEPROM (U45/U43)
22. Added power-up sequencing
23. MIO6 connected to CPLD
24. Signals EN_SFP was renamed to EN_SFP_SSD, 12V_FMC was renamed to 12V_FMC_AF, FMC12V_PG to FMCAF_12V_PG
25. Nets names F_LA02/03/04 was swapped.

REV03:
1. Signals C_LA27, P/N swapped: C_LA27_P connected to pin R10 (IO_L11P_T1U_N8_GC-_67), C_LA27_N connected to R9 (IO_L11N_T1U_N9_GC-_67) of U1 (XCZU9EG-1FFVB1156)

REV03a (17.11.2017):
1) Flash N25Q512A11E1240E changed to N25Q512A11G1240E.

REV04:
1) Added SDIO level translator TXS02612RTWR (U95) and 330 series resistors on SDIO lines from FPGA side.
2) Added user button S5 and jumper J5 (connected to U27 pin W17).
3) New FAN switches U76-78/U97-99: BTS4141N.
4) New FANs: AFB04512MA. Was added an option to use 5V or 12V (default) power rail.
5) Replaced EOL components:
   - TPS2708LDDCR -> TPS22918DBVT (U96)
   - ESD3V3ULCE6327XTSA1 -> AOZ8808DI-03 (U28)
6) New SFP+ connector: 2007492-5 instead of 1-2007492-5

REV04a:
1) Added SDIO level translator TXS02612RTWR (U95) and 330 series resistors on SDIO lines from FPGA side.
2) Added user button S5 and jumper J5 (connected to U27 pin W17).
3) New FAN switches U76-78/U97-99: BTS4141N.
4) New FANs: AFB04512MA. Was added an option to use 5V or 12V (default) power rail.
5) Replaced EOL components:
   - TPS2708LDDCR -> TPS22918DBVT (U96)
   - ESD3V3ULCE6327XTSA1 -> AOZ8808DI-03 (U28)
6) New SFP+ connector: 2007492-5 instead of 1-2007492-5

Title:  TEB0911 - REVISION CHANGES
A4  Number:  TEB0911  ZU15EGE  Rev.  04
Date:  18.09.2018  Copyright:  Trenz Electronic GmbH
Filename:  Revision_changes.SchDoc
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