TEB0911 - FPGA B504

Title: ZU_PSDDR.SchDoc

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Capacitors suitable for ZU9EG, ZU15EG
RESETN pin should be held LOW until both supplies become stable.
M.2 NGFF SMD-Abstandsbolzen - M3 - 1.5mm
The image contains a schematic diagram of an I2C system. The diagram includes various components and connections, such as VCC, GND, SCL, SDA, PS_1V8, and other elements typical of an I2C system. The schematic shows connections and labels for components like R194 (470kΩ), R195 (10kΩ), C290 (470μF), and others. The text on the diagram includes addresses like 0x77 (0b1110111x) and 0x51 (0b1010001x), indicating EEPROM and other memory locations. The diagram also shows connections for USB, CPLD, PLL, and other relevant components of the system.
REV02:
1. 2 CPLDs replaced with LCMXO2-7000HC-4FG484C (U27)
2. Single SFP connector removed. MGT lanes B129, TX/RX, 1 connected to FMC F
3. DCDC U45 (power supply of 2xSFP and 1xSFP connectors) removed. 2xSFP powered by U11.
4. HDMI lane B505_TX2 connected to DPLP_TX and lane B505_TX3 to DPLP_TX
5. Supervisor U69 TPS3106633 replaced with TPS3106E09
6. U17 (S5345): IN_SEL0/1 disconnected from CPLD and connected to GND
7. Added new clock source U57 (SDIO9AI-73-XXS-25.000000E). Connected to CPLD. Not fitted
8. 12C pull-ups R154/R155: changed from 4.7k to 1.5kOhm
9. FAN: R285, R330, R260 changed to 27K (F*SENSE)
10. Added fuse F2 (4A). Fuse F1 (1.85A) “not fitted”
11. C534 (PWR_IN_24V/GND) deleted
12. Removed clock loop-back OUT9PN - IN29PN (U17, S5345)
13. OUT7 (P) of U17 (clock source S5345) connected to CPLD U27 Bank 5.
14. Signal SD Card detect SD_CD connected to CPLD. MIO45 connected to CPLD
15. Signals FMC*_PG_C2M(M2C) pulled-up to 3.3VSB (was FMC*_3V3)
16. CLK_OUT U15 (USB PHY), serial resistor value R13 changed from 33 to 0 Ohm
17. EN5311QI. Cout value changed from 22uF to 10uF
18. ROM optimization
19. Added connections from CPLD to FMC A and F (x_LA06_SC - x_LA33_SC)
20. Not EN_VCCINT connected also to DCDC U31 (5V_SYS_PL) and U46 (5V_SYS_PS)
21. Added 2 24F EEPROM (U45/U45)
22. Added power-up sequencing
23. MIO6 connected to CPLD
24. Signals EN_SFP was renamed to EN_SFP_SSD. 12V_FMC was renamed to 12V_FMC_AF, FMC12V_PG to FMC艽AF_12V_PG
25. Nets names F_LA02/03/04 was swapped.

REV03:
1. Signals C_LA27_P/N swapped: C_LA27_P connected to pin R10 (IO_L11P_T1U_N8_GC_67), C_LA27_N connected to R9 (IO_L11N_T1U_N9_GC_67) of U1 (XCZU9EG-1FFVB1156)

REV03a (17.11.2017):
1. Flash N25Q56A1HE1240E changed to N25Q512A11G1240E.

REV04:
1. Added SMD0 level translator TXS02612RTWR (U35) and 33Ω series resistors on SMD DIO lines from FPGA side.
2. Added user button S5 and jumper J5 (connected to U27 pin W17).
3. New FAN switches U76-78/U97-99: BFT4411N
4. New FANs: AB01051.2MA. Was added an option to use 5V or 12V (default) power rail.
5. Replaced EOL components:
   - TPS2702LDCCR -> TPS2219DBVT (U96)
   - ESDIV3ULC6/32TXSA1 -> AGZ080BD-03 (U28)

REV04a (30.08.2019):
1. Resistor R65 (USB VBUS) replaced by 1kΩ.