 DDR3 CK1 and DDR3_CLK were swapped
Si5338A

SiT8208AI

25 MHz

VDDO_3
VDDO_2
VDDO_1
VDDO_0

CLK_0

BANK_14
MRCC
(VCCO= 1V8 )

MGT_BANK_115
MGTREFCLK0_115

MGT_BANK_115
MGTREFCLK1_115

CL0E_CLK

PCle 8x
CONNECTOR

SI5338A

DSC1123

200 MHz

SYSTEM CLOCK
TERMINATION

DDR3_CLK

BANK_33
MRCC
(VCCO= 1V5 )

MGT_BANK_115
MGTREFCLK0_115

MGT_BANK_115
MGTREFCLK1_115

FMC
CONNECTOR

GBTCLK0_M2C

MGT_BANK_116
MGTREFCLK0_116

MGT_BANK_116
MGTREFCLK1_116

CLK0_M2C

BANK_15
SRCC
(VCCO= VADJ)

CLK1_M2C

BANK_15
SRCC
(VCCO= VADJ)

CLK2_BIDIR

BANK_13
SRCC
(VCCO= VADJ)

CLK3_BIDIR

BANK_13
SRCC
(VCCO= VADJ)

MRCC

DDL3_CLK0

DDR3_CLK1

DDR3_SOCKET

(VDD= 1V5 )

200 MHz SOCKET

DDR3

(VDD= 1V5 )

DSC1123
SYSTEM CLOCK
TERMINATION

200 MHz
CHANGES REV01 to REV02:

1) added C87, C88 4.7µF
2) C154 incremented from 27pF to 33pF
3) route 12V input from PCIe edge connector, added input power protection circuits for ATX 12V and PCIe edge connector (U23 with T1, T2 and U24 with T5, T6, resistors and capacitors), power priority switch T3, (priority for ATX)
4) added S1 (FMC_VADJ value, and JTAG_EN)
5) T4 and resistors added for reading the FMC_PRSNT_M2C value
6) U25 and capacitors added (FMC_FAN)
7) added screws for bracket
8) added 10 x FPGA LEDs D1-D10 via levelshifter (U11, U21, U22)