1
2
3
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D D
C C
B B
A A

Date: 2018-02-26

Title: CPLD

Page2 of 33

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Filename: CPLD.SchDoc
Title: TEF1001 - FMC_PWR

Type: Set as Standard (No BOM)

Title: FMC_PWR

A4 Number: TEF1001

Date: 2018-02-26

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Page 7 of 33

Filename: FMC_PWR.SchDoc
SI5338A

25 MHz

VDDO_3 VDDO_2 VDDO_1 VDDO_0

CLK_0 BANK_14
MRCC (VCCO= 1V8 )

CLK_1 MGTCLK

MGT_BANK_115
MGTREFCLK0_115

MGT_BANK_115
MGTREFCLK1_115

PCIE CLK

PCIe 8x CONNECTOR

BANK_14
MRCC (VCCO= 1V8 )

CLK1 BANK_14
SRCC (VCCO= 1V8 )

CLK2 BANK_14

CLK2_BIDIR BANK_13

CLK3_BIDIR BANK_13

BANK_15

CLK0_M2C BANK_16

MGT_BANK_116
MGTREFCLK0_116

MGT_BANK_116
MGTREFCLK1_116

CLK0_M2C

FMC CONNECTOR

GBTCLK0_M2C

GBTCLK1_M2C

CLK0_M2C

CLK1_M2C

CLK2_BIDIR

CLK3_BIDIR

DSC1123 200 MHz SYSTEM CLOCK TERMINATION DDR3 CLK

BANK_33
MRCC (VCCO= 1V5 )

DDR3_CLK0 DDR3_CLK1

DDR3 SOCKET

(VDD= 1V5 )

DDT3_CLK0 DDR3_CLK1

GGTCLK0_M2C

GBTCLK1_M2C

CLK0_M2C

CLK1_M2C

CLK2_BIDIR

CLK3_BIDIR

BANK_13

SRCC (VCCO= VADJ)

BANK_15

SRCC (VCCO= VADJ)

BANK_16

SRCC (VCCO= VADJ)
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### Revision History

**Changes from REV01 to REV02:**

1. Added C87, C88 4.7µF
2. C154 incremented from 27pF to 33pF
3. Route 12V input from PCIe edge connector, added input protection circuits for ATX 12V and PCIe edge connector (U23 with T1, T2 and U24 with T5, T6, resistors and capacitors), power priority switch T3 (priority for ATX)
4. Added S1 (FMC_VADJ value, and JTAG_EN)
5. T4 and resistors added for reading the FMC_PRSNT_M2C value
6. U25 and capacitors added (FMC_FAN)
7. Added screws for bracket
8. Added 10 x FPGA LEDs D1-D10 via levelshifter (U11, U21, U22)