DDR3 CK1 and DDR3_CLK were swapped
FROM ATX CONNECTOR
@ 75W

12V_input_A

FROM PCIe CONNECTOR
@ 25W

12V_input_B
CHANGES REV01 to REV02:

1) added C87, C88 4.7µF
2) C154 incremented from 27pF to 33pF
3) route 12V input from PCIe edge connector, added input power protection circuits for ATX 12V and PCIe edge connector (U23 with T1, T2 and U24 with T5, T6, resistors and capacitors), power priority switch T3, (priority for ATX)
4) added S1 (FMC_VADJ value, and JTAG_EN)
5) T4 and resistors added for reading the FMC_PRSNT_M2C value
6) U25 and capacitors added (FMC_FAN)
7) added screws for bracket
8) added 10 x FPGA LEDs D1-D10 via levelshifter (U11, U21, U22)