**ClassName: Bank33**

**ClassName: CLK_DDR3**

DDR3 CK1 and DDR3_CLK were swapped

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**Filename:** FPGA_BANK_33.SchDoc

**Date:** 2018-02-26

**Copyright:** Trenz Electronic GmbH

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**Title:** TEF1001 - FPGA_BANK_33

**Number:** TEF1001

**Rev.:** 02

**Date:** 2018-02-26

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**Filename:** FPGA_BANK_33.SchDoc

Page 18 of 33
Title: TEF1001_FPGA_MGT_BANKS

A4 Number: TEF1001
TEF1001-02-160-2IK
Rev. 02

Date: 2018-02-26
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Page 20 of 33

Filename: FPGA_MGT_BANKS.SchDoc
SiS8208AI 25 MHz

DSC1123 200 MHz

SYSTEM CLOCK TERMINATION

FMC CONNECTOR

Title: TEF1001 - Clock Overview

Number: TEF1001-02-160-2IK

Rev. 02

Date: 2018-02-26

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Filename: CLOCKS OVERVIEW.SchDoc
CHANGES REV01 to REV02:

1) added C87, C88 4.7µF
2) C154 incremented from 27pF to 33pF
3) route 12V input from PCIe edge connector, added input power protection circuits for ATX 12V and PCIe edge connector (U23 with T1, T2 and U24 with T5, T6, resistors and capacitors), power priority switch T3, (priority for ATX)
4) added S1 (FMC_VADJ value, and JTAG_EN)
5) T4 and resistors added for reading the FMC_PRSNT_M2C value
6) U25 and capacitors added (FMC_FAN)
7) added screws for bracket
8) added 10 x FPGA LEDs D1-D10 via levelshifter (U11, U21, U22)